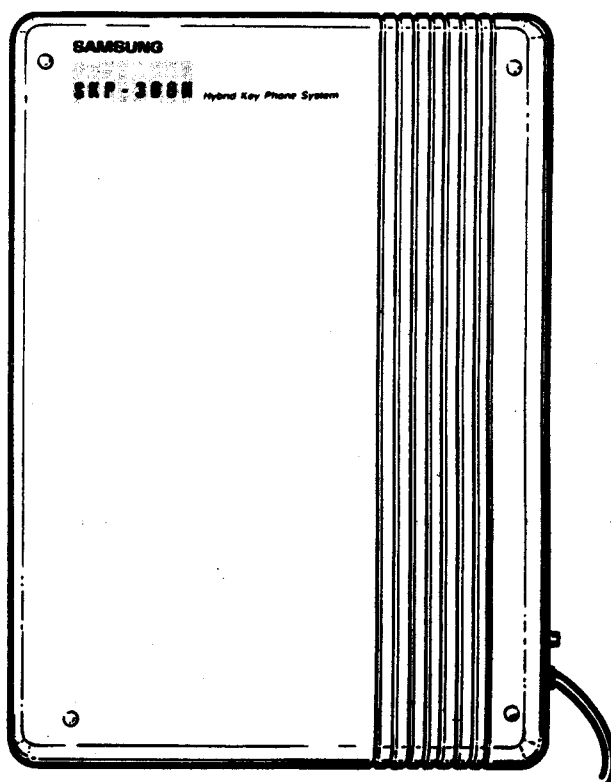


ELECTRONIC KEY/HYBRID TELEPHONE SYSTEM

SKP—308H SERVICE MANUAL



SAMSUNG

S A M S U N G

E L E C T R O N I C S C o .

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Edition 1

April 30, 1993

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P R I N T E D I N K O R E A

04/30/93

ELECTRONIC KEY/HYBRID
TELEPHONE SYSTEM

SKP - 308H

SERVICE MANUAL

Every effort has been made to eliminate errors and ambiguities in the information contained in this manual. Any questions concerning information presented here should be directed to SAMSUNG ELECTRONICS Co., 9th Fls. Joong-Ang Daily News Bldg., 7, Soonwha-Dong, Chung-ku, Seoul, Korea C.P.O. Box:2775, Tel: 82-2-751-6508,9, Fax:751-6072. SAMSUNG ELECTRONICS Co. disclaims all liabilities for damages arising from the erroneous interpretation or use of information presented in this manual.

TABLE OF CONTENTS

I.	INTRODUCTION	1
II.	GENERAL DESCRIPTION	
	1. System Overview	5
	2. Specifications	10
	3. Related Documents	14
III.	PRODUCT OVERVIEW	
	1. Order Information	17
	2. Package	19
	3. Product Dimension	27
IV.	FEATURES	
	1. Location of Controls	35
	2. Feature Description	36
V.	ASSEMBLY & DISASSEMBLY	
	1. Basic KSU Exploded View	47
	2. KSU Mechanical Partlist	49
	3. Door-phone Exploded View	50
	4. Door-phone Mechanical Partlist	51
	5. Keypad Exploded View	53
	6. Keypad Mechanical Partlist	55
VI.	ELECTRICAL INFORMATION	
	1. Circuit Description	59
	2. Voltage Chart	130
	3. Circuit Diagram	143
	4. Component Layout	153
	5. Electrical Partlist	163
	6. Component Pin Assignment	173
VII.	TROUBLE SHOOTING	
	1. Diagnostics	185
	2. Trouble Shooting	193

I . I N T R O D U C T I O N

This document is provided for the purpose of explaining all of Electrical and Mechanical informations required to maintain or repair the S A M S U N G electronic key/hybrid system S K P - 3 0 8 H.

This document starts from the GENERAL DESCRIPTION which includes system overview, specifications, and introduction of the related documents. They are helpful to understand the system architecture and characteristics. Chapter III explains ordering information, package, and product dimension, and Chapter IV includes the detail informations of the useful features.

How to assemble or disassemble the system, keyset, and door-phone is described in Chapter V and their mechanical partlists are attached. Chapter VI includes all of the electrical informations, that is, circuit description, voltage chart, circuit diagram, component layout, and electrical partlist. And, how to shoot troubles is explained in Chapter VII. Most of trouble solutions are described. Chapter VI and Chapter VII are very helpful to maintenance or repair engineer.

S A M S U N G E L E C T R O N I C S recognizes there are so many informations required to maintain or repair the system, but the following contents may be sufficient to the skillful engineer. This document with field expierences makes any engineer to an expert.

I I .

GENERAL
DESCRIPTION

1. SYSTEM OVERVIEW

SYSTEM OPERATION

SKP - 308H system is a stored program controlled electronic key/hybrid telephone system ready to use as soon as it is turned on. A powerful

8031 microprocessor operating at 11.059 MHz digitally controls all speech paths and system functions. The operating program with default memory is stored in non-volatile ROM, 27512. Customer data is stored in RAM, 62256, and protected by a Ni-Cd battery for up to thirty days' continuous loss of system power. When AC power is restored, the Ni-Cd battery is recharged.

SKP - 308H system employs a Real-Time-Clock and Space-Division-Switching of audio channels. All the trunk lines can be accessible at any time, non-blocking network, and 5 audio channels are prepared; three channels are intercom speech paths and the other two are used for tones and music.

SKP - 308H system has a maximum capacity of three telephone lines (trunks) and eight stations. Comprised of only a key service unit, electronic keysets, and conventional single line telephones, **SKP - 308H** system offers small business user's flexibility and control of telephone communications.

SYSTEM CONFIGURATION

The **KSU (Key Service Unit)** comes equipped to operate three (3) telephone lines and eight (8) stations. Station #1 is assigned for electronic keyset and stations from #2 to #8 are assigned to be used with single line telephones or keysets which are respectively selected.

The maximum number of each circuit type available in **SKP - 308H** system are listed below:

Circuit Type	Maximum Number available
Electronic Keyset	8
Single Line Telephone	7
C.O. Line (loop start)	3

SYSTEM HARDWARE

KEY SERVICE UNIT (KSU) is a single cabinet, wall mounted, plastic cased unit measuring 420mm H x 300mm W x 84mm D, and its weight is 3.8 Kg. It contains basically the following assemblies:

Power Supply Board - This board provides all the necessary DC powers from 110/220V AC power which is selectable. Also contains a charge/discharge circuit for 24V external battery backup connections and ring generator for conventional single line telephones.

Base Board - It is the main printed circuit board that contains CPU, memory, common control, and switching circuitry. Provides interfaces for telephone lines 1 through 3, stations 1 through 8, and the additional features:

- Music on Hold & Background music source
- External Paging
- Power Fail Transfers for line 1 through 2
- Door Phone with lock release contact

Also, contains memory backup battery and +24V DC regulator for relay driving.

Station 1 for keyset and the other stations for keysets or single line telephones respectively switch-selected.

DOOR PHONE/ROOM MONITOR - An optional wall mounted unit containing a call button, micro-phone, and speaker. Connects to KSU via two pairs twisted wiring. Does not take up a C.O. line or station position. Only one per system.

TELEPHONES

There are two types of telephone sets that can be connected to **SKP - 308H** system. Proprietary electronic keysets and conventional single line telephone sets.

AS - 11 SERIES electronic key telephone sets provide every user with all of the most desirable features built in. There are four kinds:

AS - 11B has the standard features listed below.

AS - 11E has the standard features plus a large one line sixteen character Liquid Crystal Display unit with easy to read.

AS - 11BV has the standard features plus Voice Message Service feature.

AS - 11EV has the standard features plus a large one line sixteen character Liquid Crystal Display unit and Voice Message Service feature.

VOICE MESSAGE SERVICE is divided to three Voice Alarm Services and two Voice Message Sending Services.

◆ AS - 11 SERIES Standard Features

- * Full speakerphone capability.
- * Each keyset comes as a desk model with reversible base wedge and handset clip for wall mounting at no extra cost.
- * Handset and base cord connectors are designed with strain relief channels for longer cord life and more static-free connections.
- * Forty (40) buttons configured as following:
 - Twelve (12) dial buttons (from 0 to #).
 - Three (3) C.O. buttons with dual color LED indicators.
 - Eight (8) DSS/BLF buttons.
 - One (1) FAX button with LED indicator, which transfers the line directly to FAX station.
 - Six (6) speed dial buttons with LED indicators.

Ten (10) feature buttons:

Function/Do Not Disturb	---	F U N C / D N D (red LED)
Transfer/Alarm	---	T R S F / A L M (red LED)
Page	---	P A G E (red LED)
Volume Down	---	▼
Volume Up	---	▲
Speaker	---	S P K (red LED)
Message	---	M S G (red LED)
Last Number Redial/Auto Redial	---	R D (red LED)
Flash	---	F L A S H (red LED)
Hold	---	H O L D (orange button, with red LED)

- * Touch-button Volume Control - Handset RX by 4 steps, Speaker-phone RX by 8 steps, and Ring tone by 8 steps.
- * Key Confirmation Tone (1000 Hz, 100 mS) in dialing.
- * One slide-type volume selectors for control Liquid Crystal Display brightness at AS-11E or AS-11EV model.
- * Convenient pull-out tray under keyset for directory information.
- * Individual external speaker connected for Individual Loud Bell Service.

AS - 3 0 SERIES can be connected to use: AS-30B, AS-30E, AS-30BV, AS-30EV.

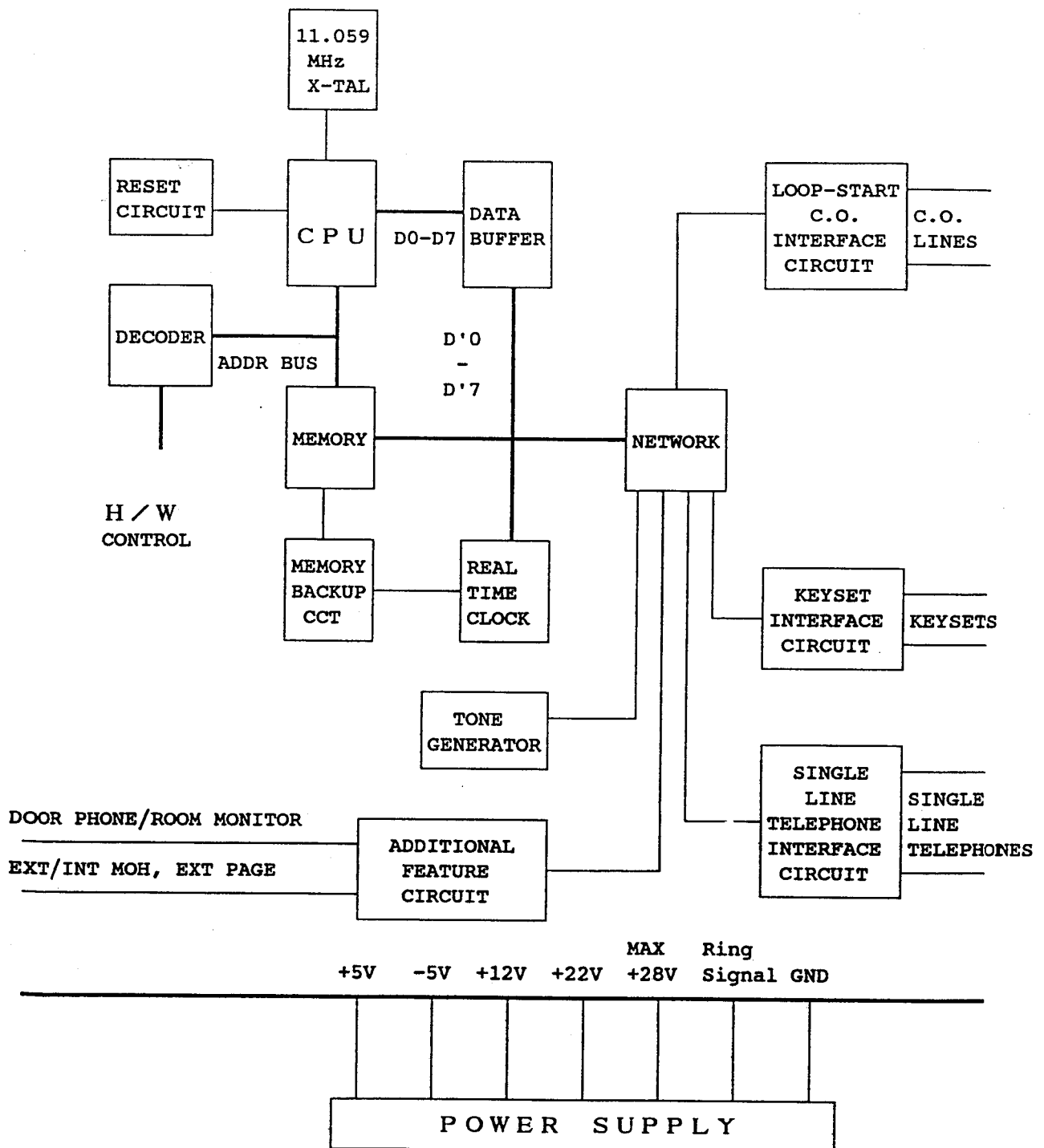
SKP 8 1 6 H KEYSETS can be connected to use: Standard type and Executive type keysets.

SKP 3 0 8 / 8 1 6 KEYSETS can be connected to use: Standard type and Executive type keysets.

All keysets listed above are fully "Hearing Aid Compatible" as required by FCC part 68 Rules.

CONVENTIONAL TELEPHONES - Any industry-approved single line telephone using one pair (two wire) tip and ring circuitry may be connected to a single line station port in the system. The ringer equivalency of any such phone must not exceed 5.0B or damage to the system may result.

SYSTEM BLOCK DIAGRAM



2. SPECIFICATIONS

SYSTEM CAPACITY

3 CO/PABX lines (Loop start, 600 ohms)
- Non-blocking connections
1 up to 8 keysets
Up to 7 single line telephones

5 speech paths
- 3 intercom speech paths
- 1 audio channel for system call progressive tones
- 1 audio channel for music (Internal or External)

1 door-phone with lock release contact
3 DTMF receivers
1 DTMF sender
1 call progressive detector
1 external page

Automatic Power Failure Transfer Circuits, 2 telephone lines

POWER SPECIFICATIONS

AC Input:	Switch-Selectable 110 or 220 VAC at 50/60 Hz 90 - 130 VRMS Acceptable at 110 Switch 180 - 260 VRMS Acceptable at 220 Switch
Power Consumption:	40.0 Watts maximum
Max Current Draw:	1.0 AMP
Ring Generator:	80 VRMS 20 Hz
Battery Back-Up Supply:	24 VDC Batteries rating not less than 6 AH but not more than 40 AH

ENVIRONMENTAL LIMITS

Operating Temperatures:	0 °C - 45 °C (18 °C - 25 °C recommended)
Operating Humidity:	10 % - 90 % (without condensation)

CABLE REQUIREMENTS

Electronic Set:	2 pair twisted, 400m 24AWG maximum
Single Line Telephone:	1 pair twisted, 400m 24AWG maximum
Door Phone:	2 pair twisted, 100m 24AWG maximum

PHYSICAL DIMENSIONS & WEIGHTS

Key Service Unit:	420 mm H x 300 mm W x 84 mm D, 3.8 Kg
Keyset:	229 mm H x 195 mm W x 91 mm D, 0.95 Kg
Door Phone:	158 mm H x 89 mm W x 41 mm D, 0.23 Kg

External Music Source Input:	Impedance 600 ohms, 350 mV
External Amplifier Output:	Impedance 600 ohms, 1.24 Vrms

ELECTRICAL CHARACTERISTICS

This section says the standard characteristics, and some of them may be changed accroding to the related telecommunication network.

Crosstalk:	81 dB
Off-Hook, DC Resistance:	215 Ω
Capacitance:	0.4 μ F
On-Hook, Capacitance:	0.8 μ F
Impedance:	13.5 k Ω
Insulation Resistance:	1.2 G Ω
Dial Pulse, Pulse Speed	10.1 PPS
Make Rate	33.8 %
Inter-Digit Time	600 mS in default (may be changed up to 9900 mS by user-programming.)
DTMF, Low Frequency Group	697, 770, 852, 941 Hz $\pm$ 1.5 %
High Frequency Group	1209, 1336, 1477 Hz $\pm$ 1.5 %
Low Frequency Level	- 5.7 dBm $\pm$ 0.5
High Frequency Level	- 8.1 dBm $\pm$ 0.5
Signal Duration	100 mS in default (may be changed up to 9900 mS by user-programming.)
Inter-Digit Time	100 mS
Trunk, Average Sending Level	- 16.7 dBm
Maximum Sending Level	- 5.4 dBm
Out-of-Band Noise (4 - 8 KHz)	- 35 dBm below
(8 - 12 KHz)	- 50 dBm below
(12 - 50 KHz)	- 62 dBm below

AUDIBLE AND VISUAL INDICATIONS

LED	STATUS	LINE STATUS
C.O. line LED (Green/Red)	OFF Flash green every 0.1 Sec Flash green every 0.5 Sec Steady Green Steady Red	Idle Receiving C.O. line call / C.O. line is on Exclusive Hold C.O. line is on Universal Hold The station is using this C.O. line Other station is using this C.O. line
Intercom LED (Red)	OFF Flash every 0.1 Sec Flash every 0.5 Sec Steady-ON	Idle Receiving station call / Station is on Exclusive Hold Station is on Universal Hold Busy
FUNC/DND LED (Red)	Flash every 0.5 Sec Steady-ON	In Night Ring Service mode In Do Not Disturb mode
TRSF/ALM LED (Red)	Steady-ON	Alarm is set
PAGE LED (Red)	Steady-ON	In paging
SPK LED (Red)	Flash every 0.1 Sec Steady-ON	During set initializing. - Data communication to KSU fails. Speaker-phone mode indication, which is not prior to handset mode.
MSG LED (Red)	OFF Flash every 0.1 Sec Steady-ON	No message left Message left from other station Message to other station
RD LED (Red)	Flash every 0.5 Sec Steady-ON	During auto-redial During redial
FLASH LED (Red)	Flash during the flash time	During Flash the C.O/PABX line
HOLD LED (Red)	Steady-ON Flash every 0.1 Sec	During HOLD operation Button sticking indication during initializing the keyset.
FAX LED	OFF Flash every 0.5 Sec Steady-ON	All of FAX stations are free. One FAX station is busy when two stations are assigned to FAX's. All of FAX stations are in use.
SD LED (Personal Speed Dial, Red)	Steady-ON	In use

AUDIBLE AND VISUAL INDICATIONS

TONE	STATUS Dual Tone (350 Hz + 420 Hz)
Dial Tone	[Continuous] or [1 Sec. ON, 0.25 Sec. OFF] Selected by User-Programming. (Program 28) - Handset is lifted or SPK button is pressed - HOLD button is pressed while talking to station or C.O.
Busy Tone	0.5 Sec. ON, 0.5 Sec. OFF - Selected C.O. line or intercom line is busy
Ring Back Tone	1 Sec. ON, 2 Sec. OFF - When making an intercom call
Transfer Tone (Conference Tone Function Tone)	0.2 Sec. ON, 0.2 Sec. OFF - Making a Transfer of C.O. line or station - FUNC/DND button is pressed while talking - Making a Conference - PAGE button is pressed
Error Tone	0.5 Sec. ON, 2.5 Sec. OFF - When making an intercom call or C.O. line access which is not connected
Confirm Tone	2 Sec. ON, once - When a call reservation is made
Burst Tone	0.2 Sec. ON, 0.2 Sec. OFF, three times, KEYSET ONLY (keyset ring) - In Diagnostic, a button is pressed
R I N G	Ring tone for keyset & Ring signal for single line telephone
C.O. line ring	1 Sec. ON, 2 Sec. OFF - When a C.O. line is ringing
Station ring	0.4 Sec. ON, 0.2 Sec. OFF, 0.4 Sec. ON, 2 Sec. OFF - When a station is receiving a call
Doorphone ring	0.2 Sec. ON, 0.2 Sec. OFF - When a door phone call is ringing
Alarm ring	0.5 Sec. ON, once, KEYSET ONLY - A station ring when busy

3 . R E L A T E D D O C U M E N T S

A. SKP-308H INSTALLATION & PROGRAMMING MANUAL

This document includes how to install the system and its additional equipments, how to change the useful features by user-programming, and some important electrical information. Supplied with the basic KSU in default.

B. SKP-308H KEYPHONES & STANDARD PHONE USER'S GUIDE

This document explains how to use AS-11 series or single line telephones connected to SKP-308H system. Supplied with each Keyset in default.

I I I .

PRODUCT
OVERVIEW

1 . ORDER INFORMATION

This information is based on the standard products. For the specific country, the order-number may be changed to the other name.

SYSTEM ORDERING

KP 308HMUSA Basic KSU

- One 308 Base Board
- One Power Board
- One Installation & Programming Manual
- One Rack Ass'y
- One spare AC Fuse (250V 1A, slow-blow)
- One spare Battery Fuse (250V 3A, slow-blow)
- One Package

KP 308HBCOINT

Additional parts for CO installation

KP 816HBDPHSCHA One Door-phone

Master Carton includes 12 unit packages

KP 308HBMDFUSA

One A-type MDF

Master Carton includes 12 A-Type unit packages (6 products)

KEYSET ORDERING

KP 308HSUSA AS-11B

One AS-11B Main Set with Bracket
One Handset (Two Dynamic Units, Modular Connection)
One Handset Cord (4 pin, 300 mm long)
One Line Cord (4 pin, 3 m long, Double-side Modular Plug)
Two spare DSS Guide Papers

Master Carton includes 8 unit packages

KP 308HSWLUSA AS-11E

One AS-11E Main Set with Bracket
One Handset (Two Dynamic Units, Modular Connection)
One Handset Cord (4 pin, 300 mm long)
One Line Cord (4 pin, 3 m long, Double-side Modular Plug)
Two spare DSS Guide Papers

Master Carton includes 8 unit packages

KP 308HSVUSA AS-11BV

One AS-11BV Main Set with Bracket
One Handset (Two Dynamic Units, Modular Connection)
One Handset Cord (4 pin, 300 mm long)
One Line Cord (4 pin, 3 m long, Double-side Modular Plug)
Two spare DSS Guide Papers

Master Carton includes 8 unit packages

KP 308HSWLVUSA AS-11EV

One AS-11EV Main Set with Bracket
One Handset (Two Dynamic Units, Modular Connection)
One Handset Cord (4 pin, 300 mm long)
One Line Cord (4 pin, 3 m long, Double-side Modular Plug)
Two spare DSS Guide Papers

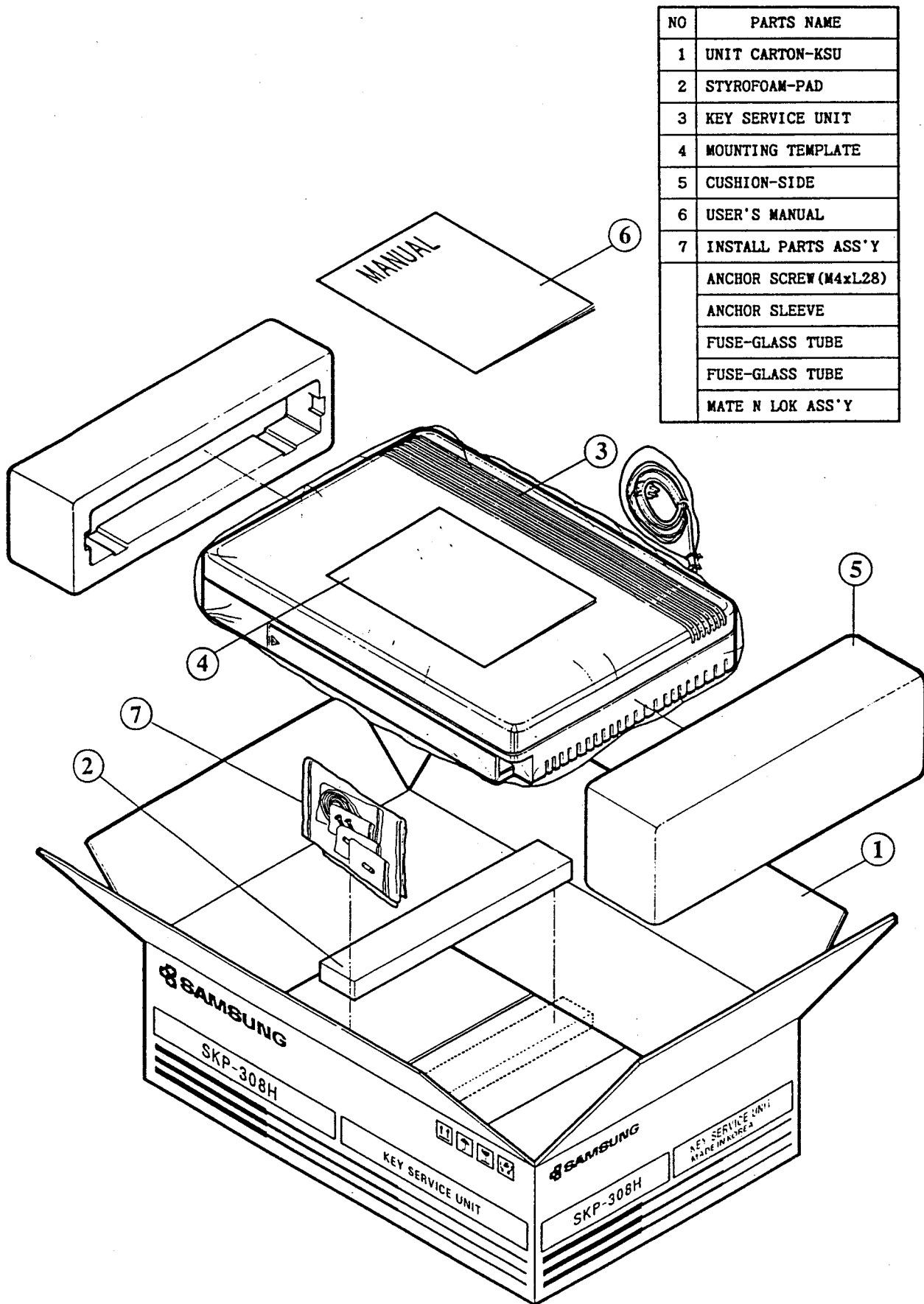
Master Carton includes 8 unit packages

2 . P A C K A G E

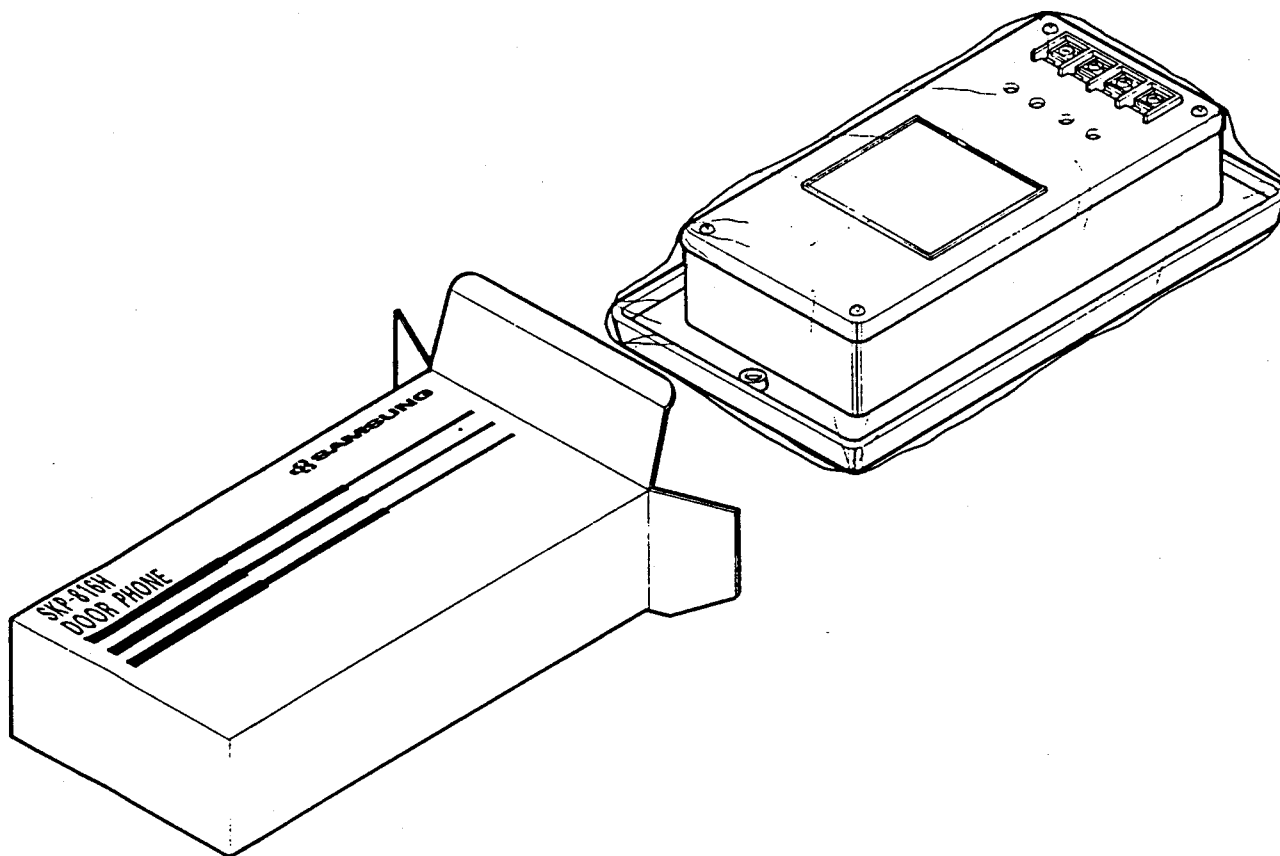
CONTENTS

A.	Basic KSU Package	20
B.	Door-phone Unit Package	21
C.	Door-phone Master Carton	22
D.	A-Type MDF Unit Package	23
E.	MDF Master Carton	24
F.	Keyset Unit Package	25
G.	Keyset Master Carton	26

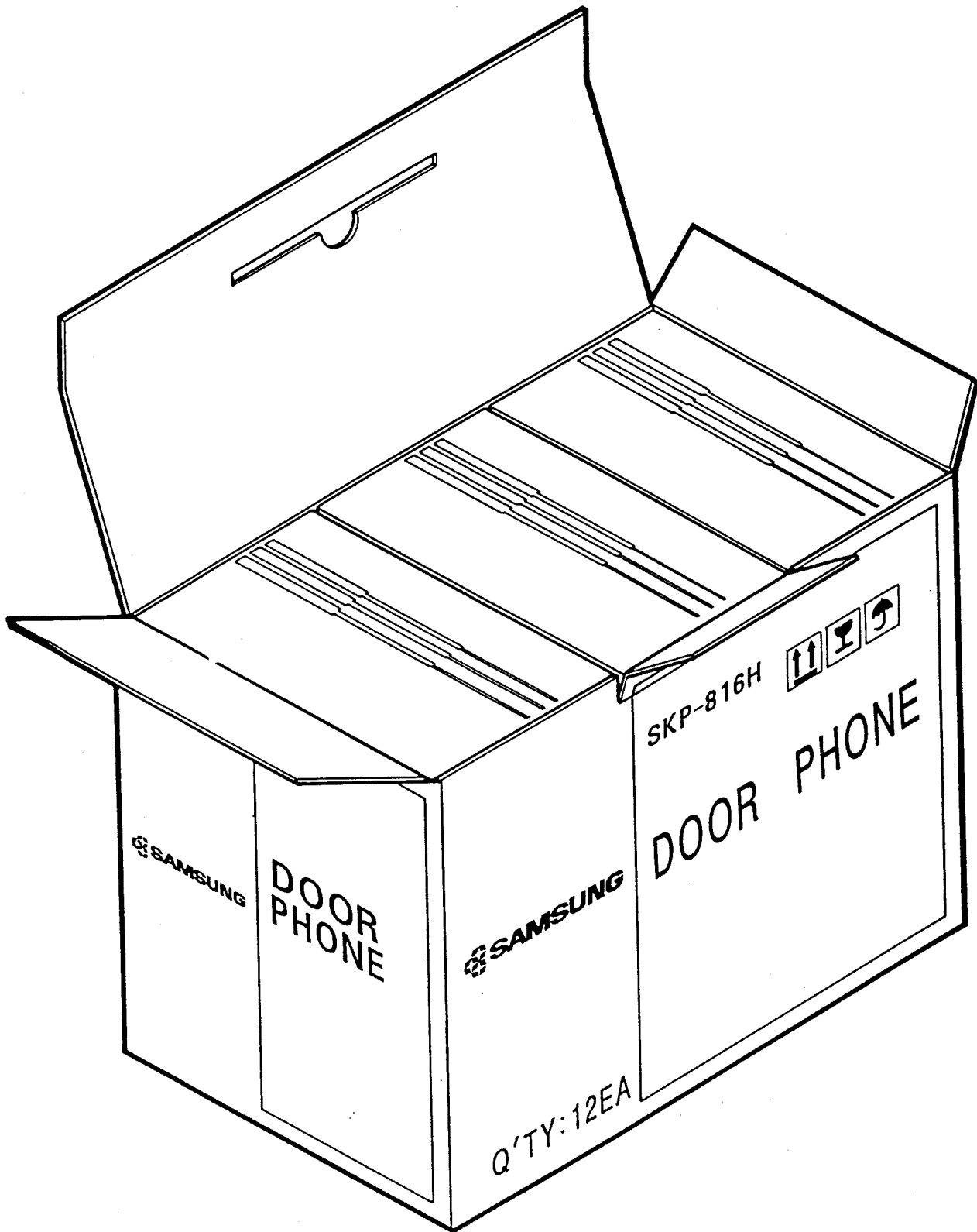
A. BASIC KSU PACKAGE



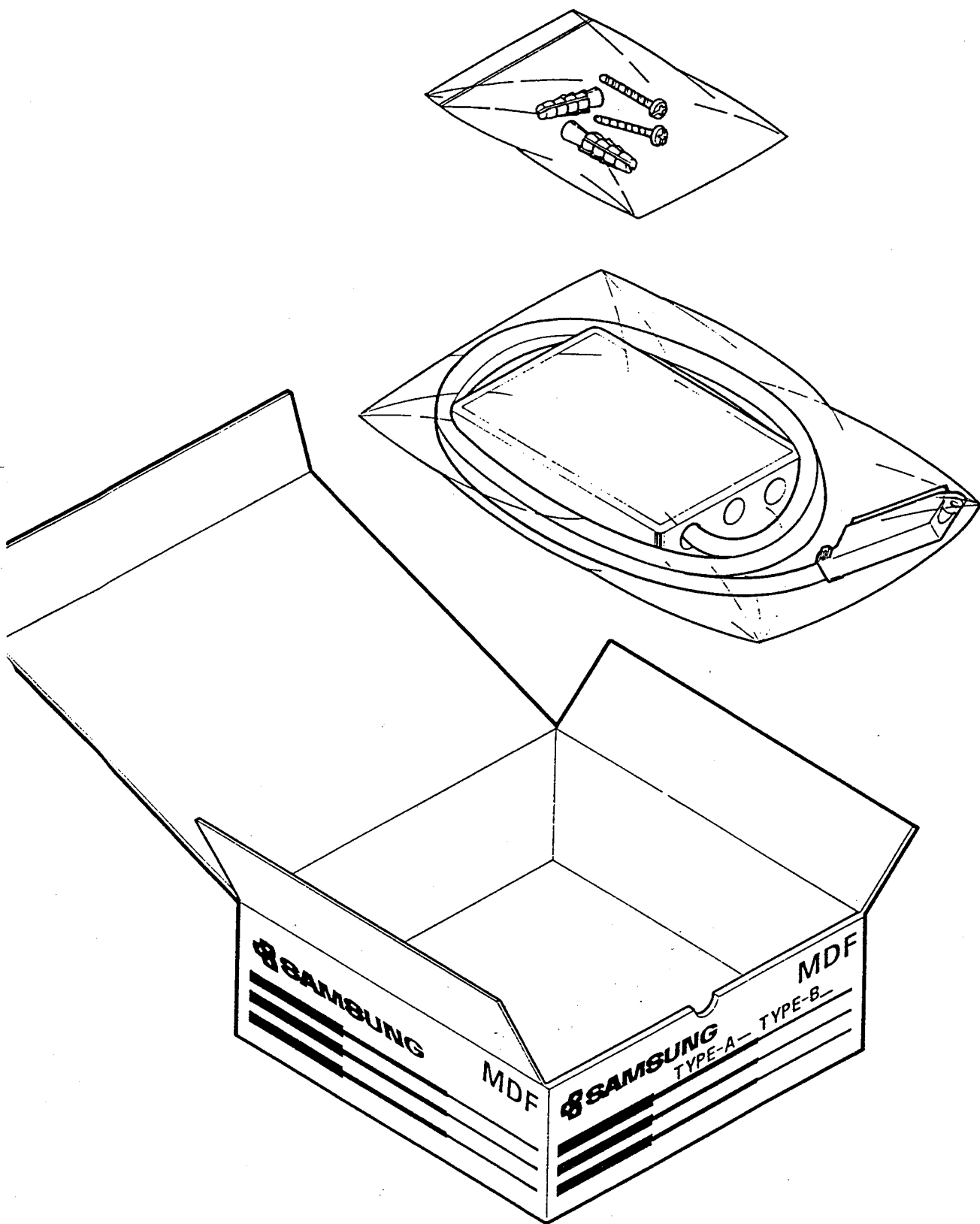
B. DOOR-PHONE UNIT PACKAGE



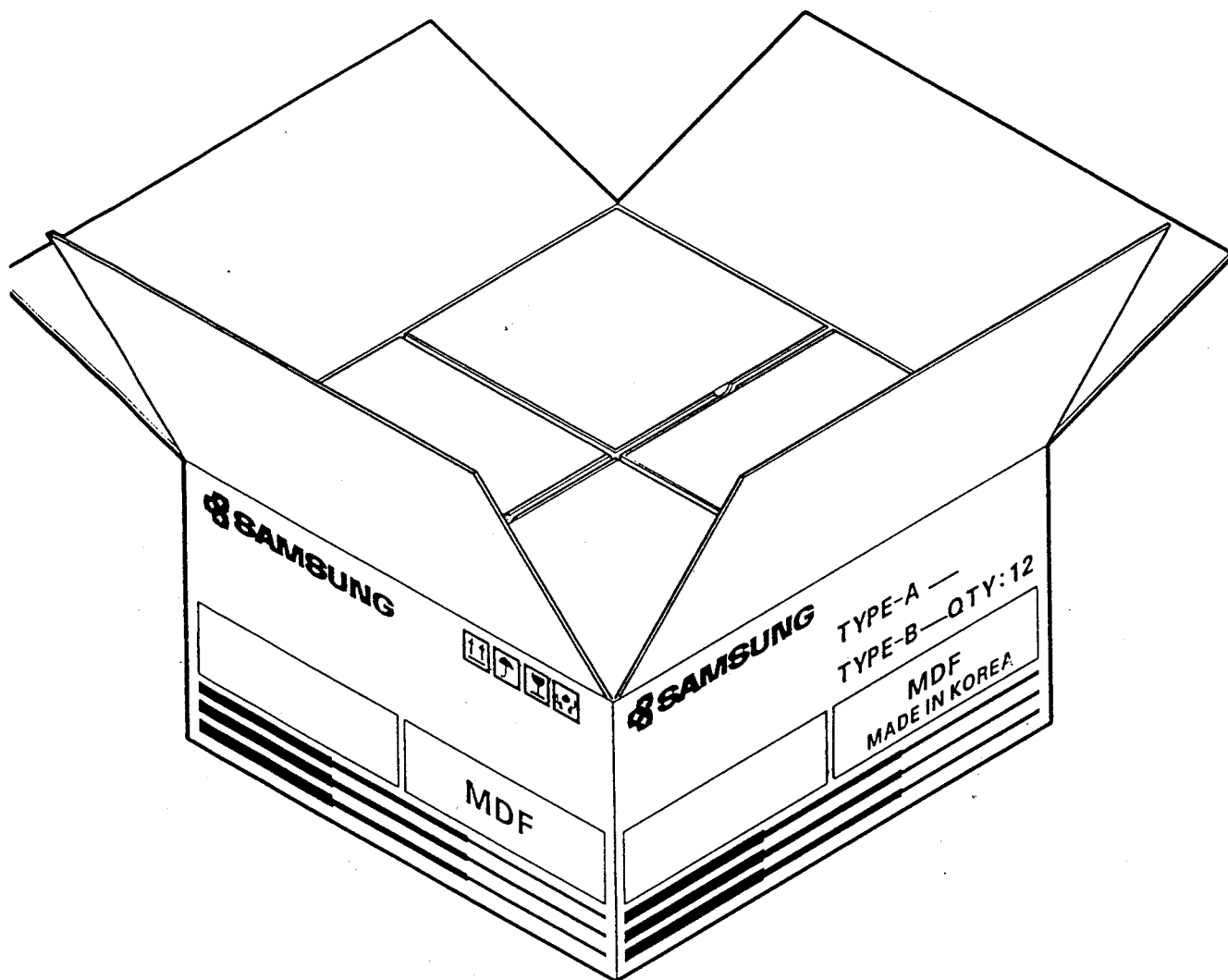
C. DOOR-PHONE MASTER CARTON



D. A-TYPE MDF UNIT PACKAGE

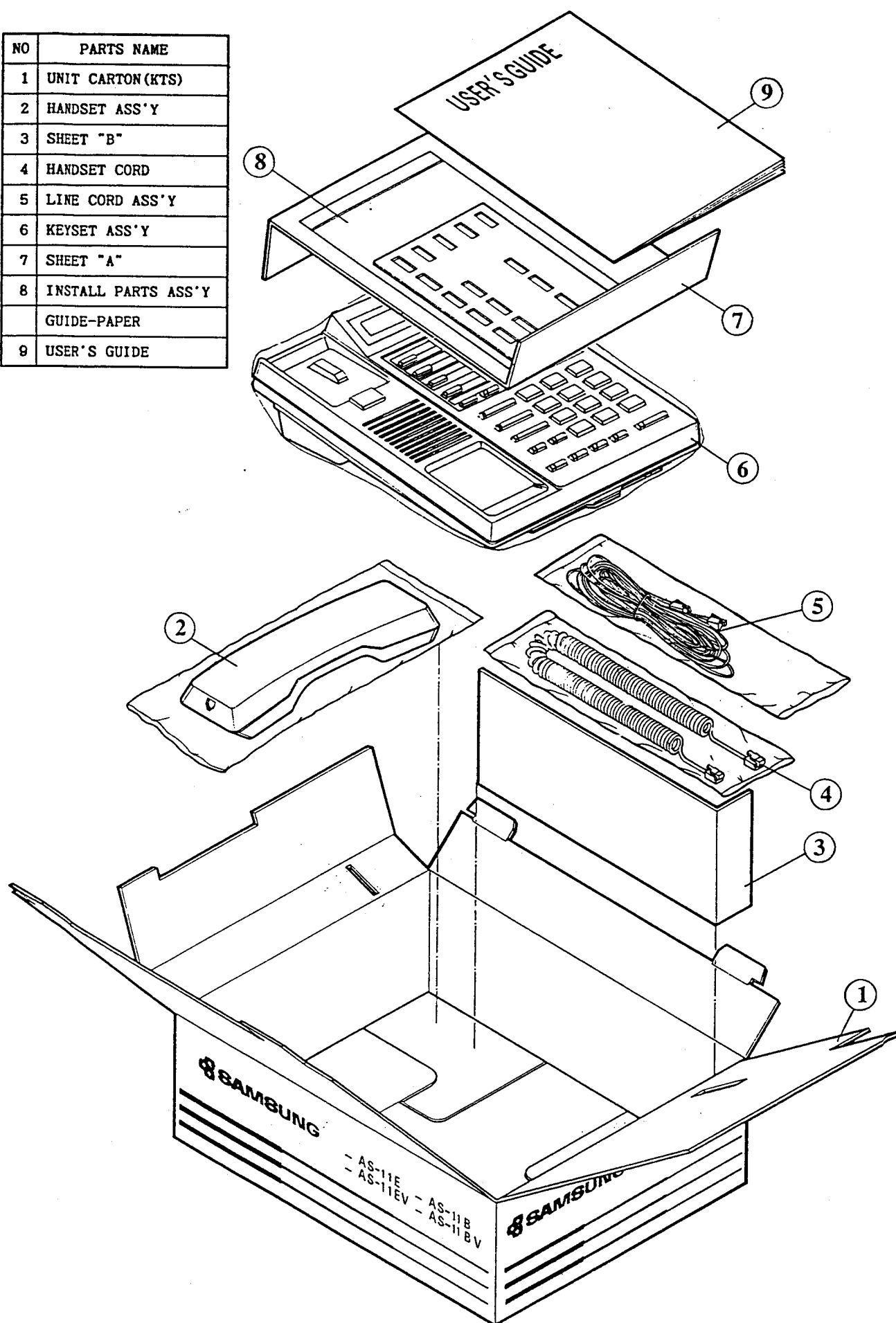


E. MDF MASTER CARTON

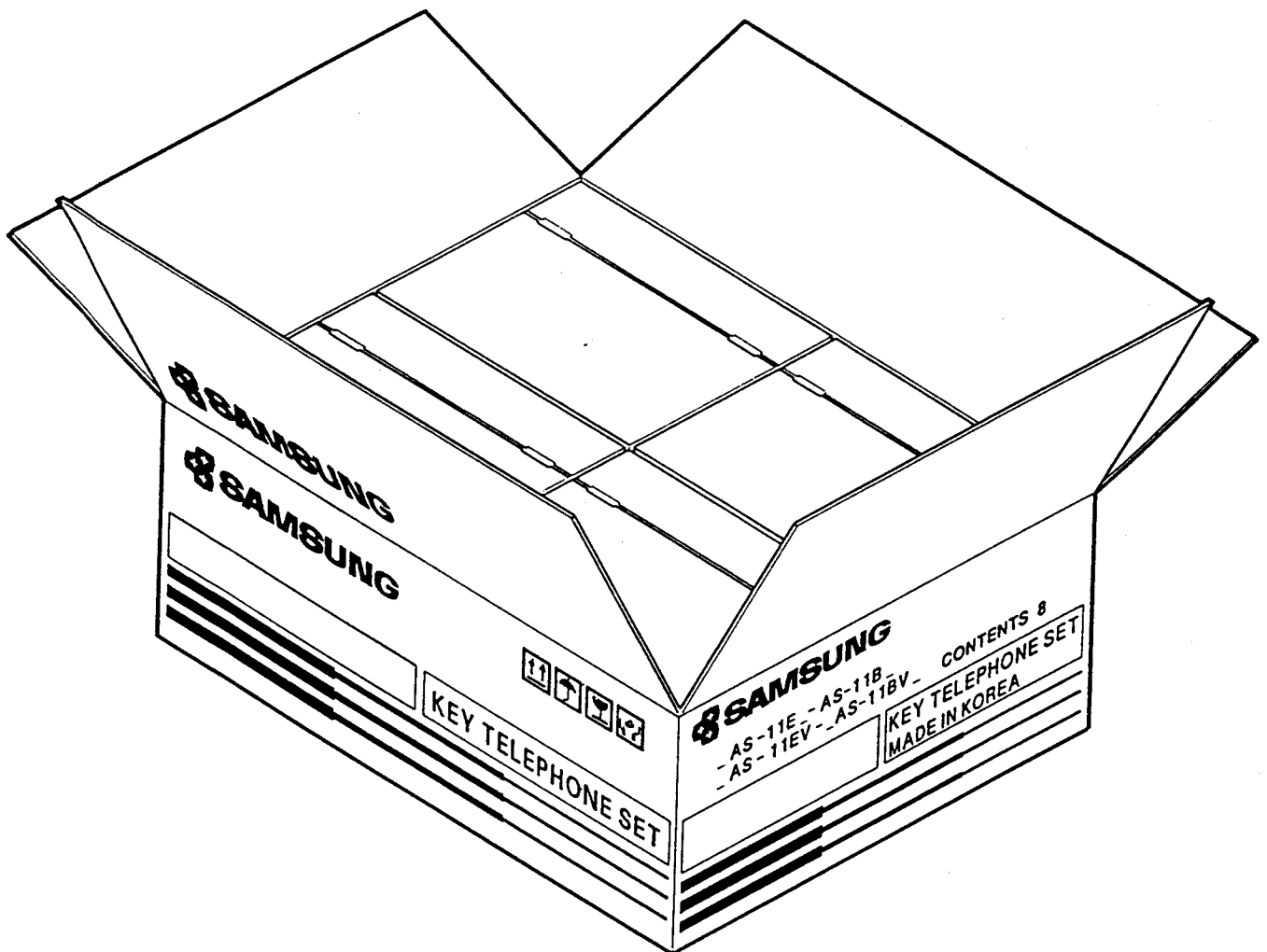


F. KEYSSET UNIT PACKAGE

NO	PARTS NAME
1	UNIT CARTON (KTS)
2	HANDSET ASS'Y
3	SHEET "B"
4	HANDSET CORD
5	LINE CORD ASS'Y
6	KEYSET ASS'Y
7	SHEET "A"
8	INSTALL PARTS ASS'Y
	GUIDE-PAPER
9	USER'S GUIDE



G. KEYSET MASTER CARTON

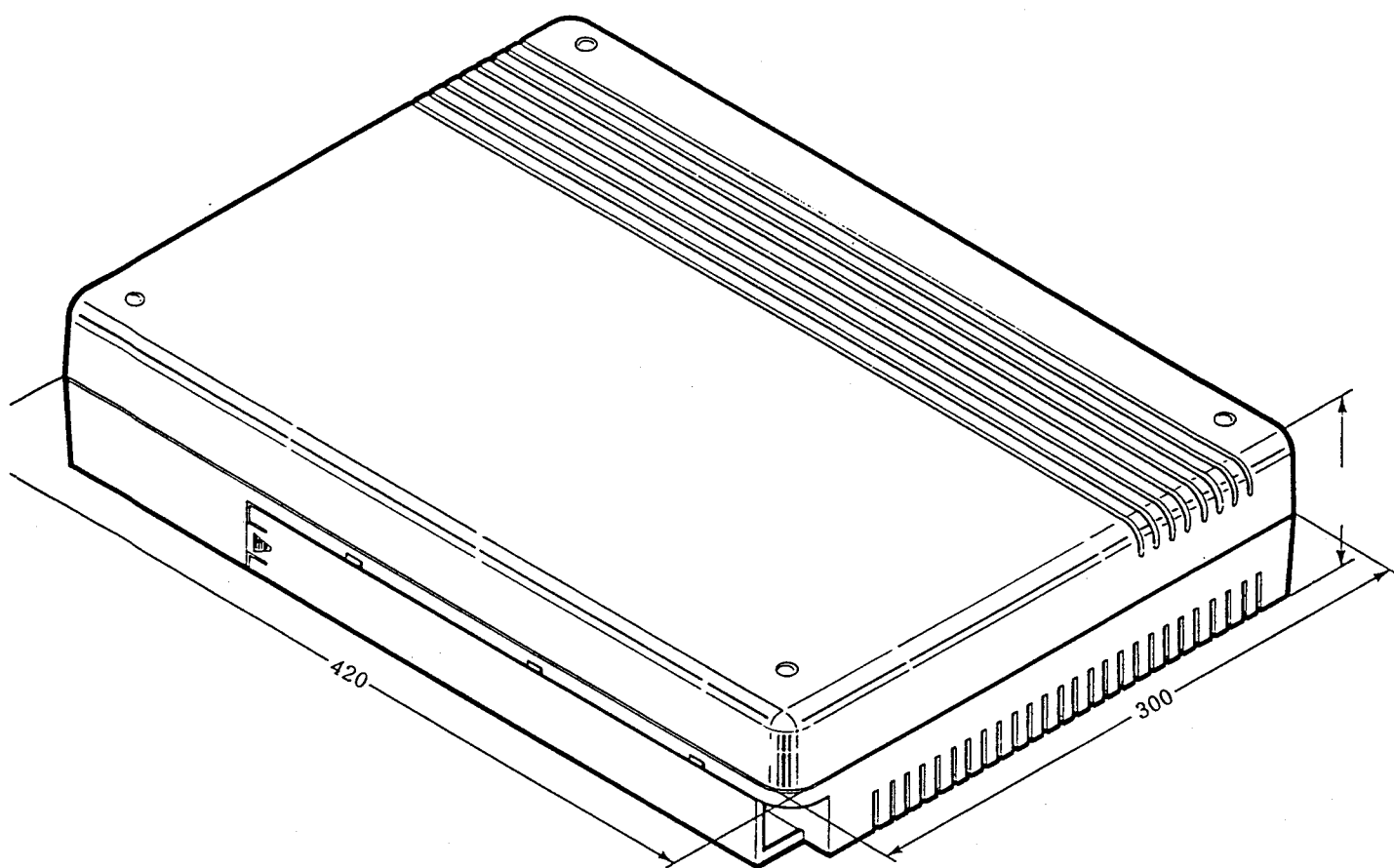


3. PRODUCT DIMENSION

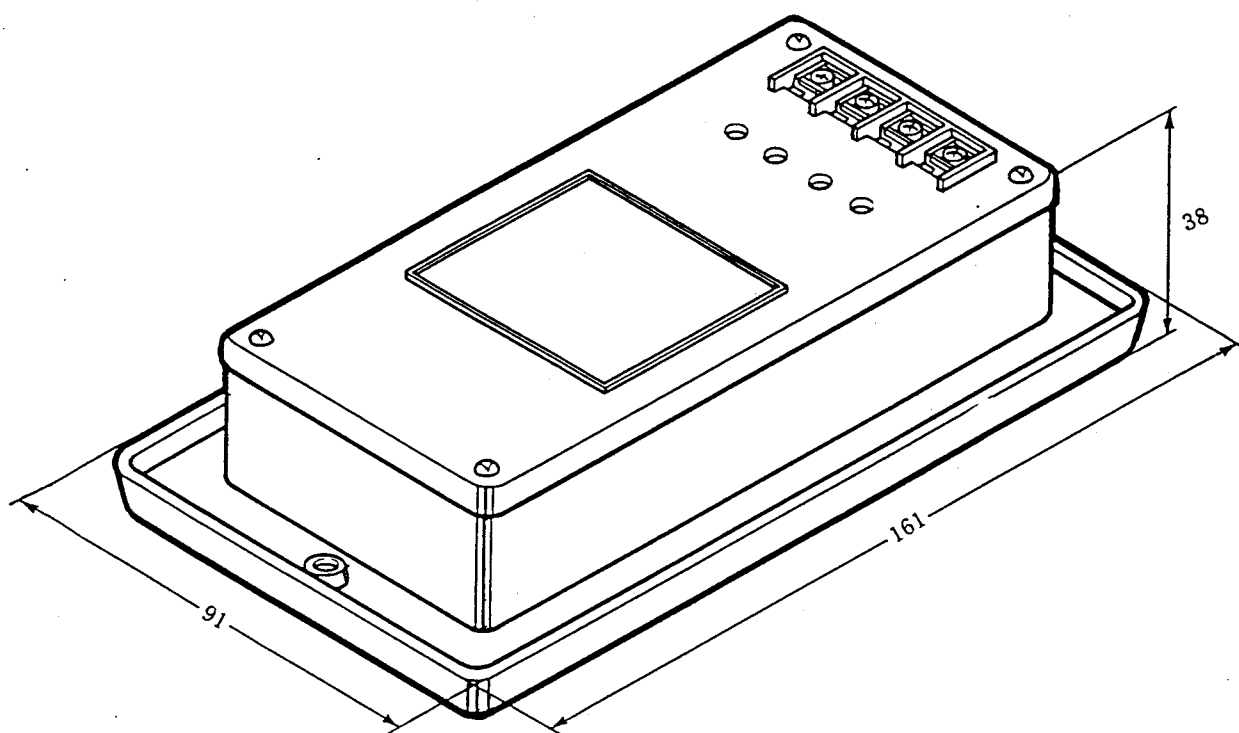
CONTENTS

A.	Basic KSU Dimension	28
B.	Door-phone Dimension	29
C.	A-Type MDF Dimension	30
D.	Keyset Dimension	31

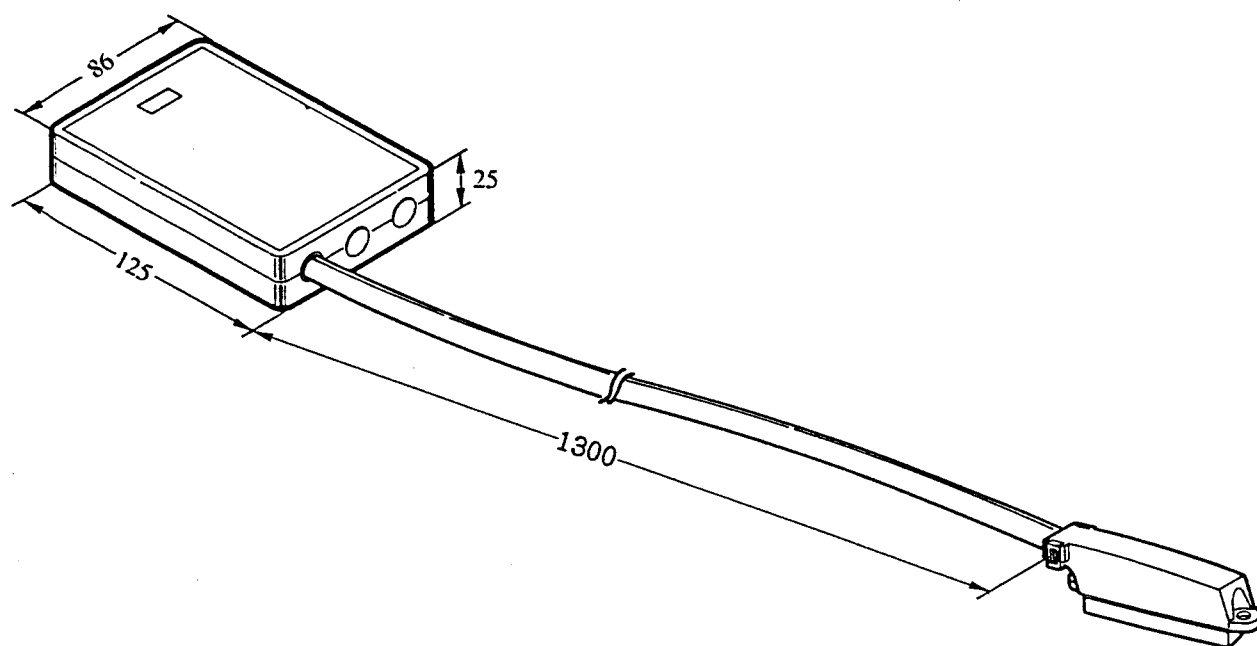
A. BASIC KSU DIMENSION



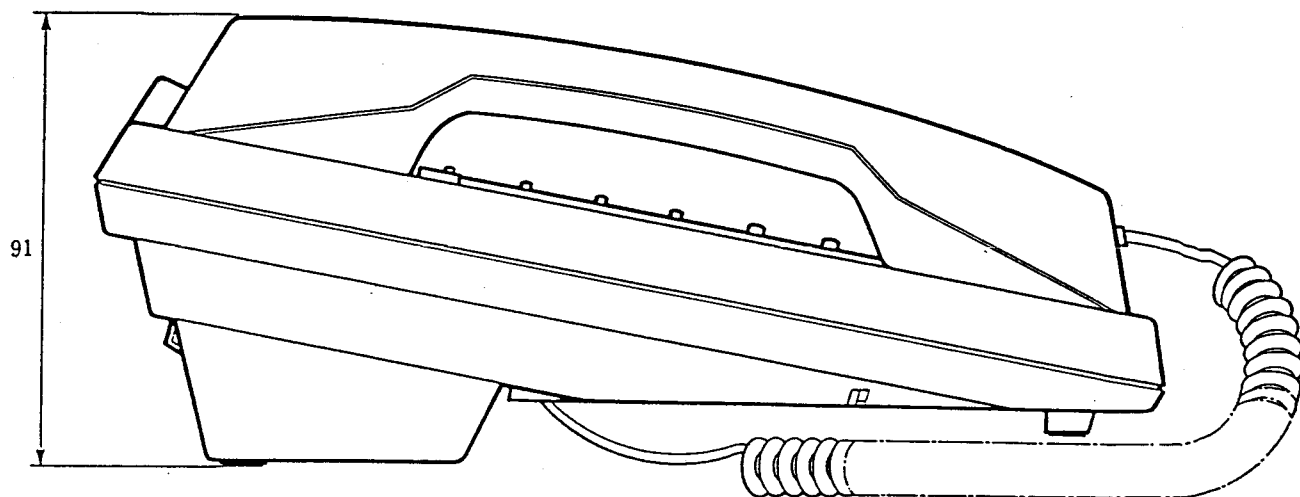
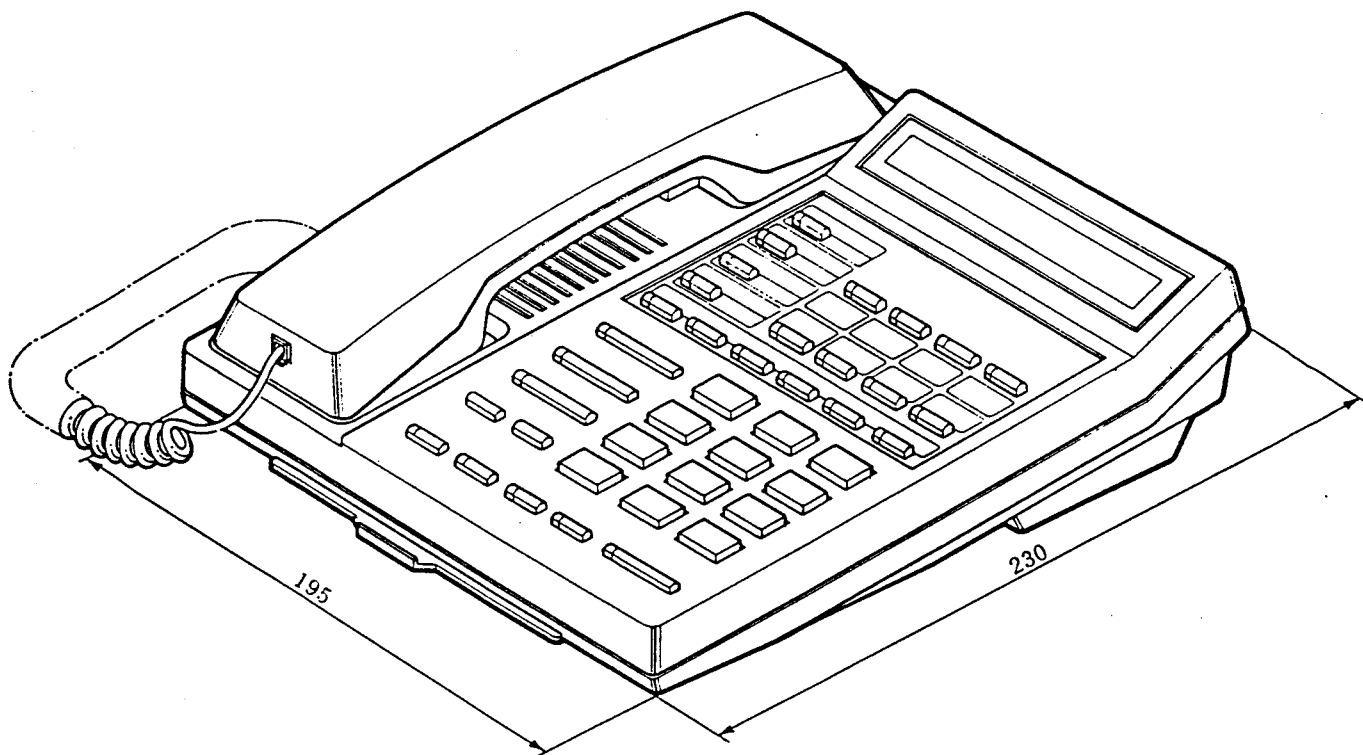
B. DOOR-PHONE DIMENSION



C. A-TYPE MDF DIMENSION



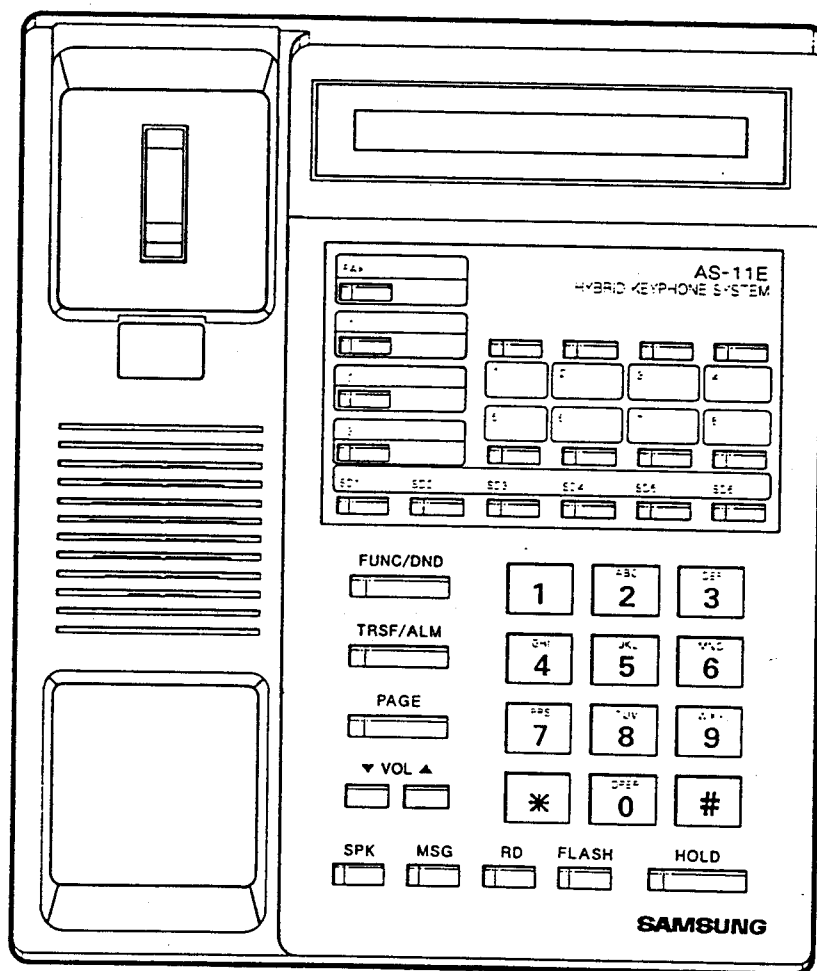
D. KEYSET DIMENSION



I V .

FEATURES

1. KEYSET LOCATION OF CONTROLS



2. FEATURE DESCRIPTION

Most of important features in SKP - 308H system are described with their definitions and the necessary informations which are helpful to maintain the system and to understand the system operation.

AUTO TIMER

For an outgoing call, Auto Timer may be activated by user-programming (Program code 65). In eight (8) seconds after outside line access, timer will be automatically activated, which will be shown at the keyset display.

Related Control : Program Code 65 (Auto Timer)

AUTOMATIC HOLD

During an outside call, pressing PAGE, TRF/ALM, or any DSS button puts the call automatically on hold.

AUTOMATIC RECALL

Held, or transferred calls not answered in a programmable period of time will recall the originating station. If not answered then they will recall to the operator.

BACKUP BATTERY, MEMORY

The system is equipped with a memory back-up battery that prevents loss of customer data base stored in RAM during power failure. 3.6V 60 mAH NiCd battery is used in default. It backs up the data memory RAM and Real Time Clock. This memory back-up is turned off at the factory before shipping to preserve battery life. Immediately after installation of the KSU, switch "BACK-UP" ON. The battery will be recharged when power restored.

The customer data base should be cleared by Switch "BACK-UP" control or by User programming (Program code 25) if the configuration of the running system is changed.

Related Control : Memory Backup Switch "BACK-UP" on Base Board

BACKUP BATTERY, SYSTEM

The system will continue the full operation during Power Failure when a 24VDC battery is connected. Any NiCd or car battery (rechargeable) can be connected if its rating is not more than 40AH and not less than 6AH.

Be careful to handle the external battery to avoid personal injury or system damage. Connect or disconnect the battery during AC power ON. That is less dangerous.

BEHIND PBX

Trunk lines may be programmed for behind PBX use to allow for hookflash. Hook flash time for PBX may be adjusted. The system does not restrict any Toll regardless of the station class on the PBX-assigned trunk. Sending a hook flash to PBX can be accomplished by pressing FLASH button or Function ID access.

Related Control : Program Code 43 (CO or PBX Line)
 Program Code 51 (PBX Flash Timing)

BOSS/SECRETARY

Maximum three (3) stations can be assigned to Bosses for one Secretary. This feature is different from Hot line. It operates as a specific DSS. A boss station can not be assigned to a secretary.

Related Control : Program Code 73 (Boss/Secretary Assignment)

CHAIN DIALING

Users may dial manually the additional digits following a speed dial call or chain together as many speed dial numbers as required.

CONFERENCE

A maximum of five (5) party conference may be accomplished without any gain compensation, in any combination of outside lines and intercom stations in any order.

DAY/NIGHT RING ASSIGNMENT	
1	2
3	4
5	6
7	8
9	10
11	12
13	14
15	16
17	18
19	20
21	22
23	24
25	26
27	28
29	30
31	32
33	34
35	36
37	38
39	40
41	42
43	44
45	46
47	48
49	50
51	52
53	54
55	56
57	58
59	60
61	62
63	64
65	66
67	68
69	70
71	72
73	74
75	76
77	78
79	80
81	82
83	84
85	86
87	88
89	90
91	92
93	94
95	96
97	98
99	100

Each C.O. line may be programmed to ring the selected stations during day operation and the different stations when the system is placed in night service. Day/night service mode can be assigned in the Attendant station with toggling DND mode. DND mode of Attendant activates the system to night service mode.

Related Control : Program Code 70 (Attendant Assignment)
Do Not Disturb in User's Guide

DOOR LOCK RELEASE

After answering a call from the door phone or making a call to the door phone, dialing "1" will give a contact closure to operate a customer provided electronic door lock. The contact closure time is programmable from 0.1 to 9.9 seconds (Program code 58). The system is equipped with one door-phone and co-operated door lock release in Basic KSU.

Related Control : Connecting Door-phone and Lock Control
Program Code 58 (Door Open Time)

DOOR PHONE / ROOM MONITOR

One door-phone may be connected to Basic KSU at maximum. Pressing the button of door-phone makes a call to the related stations programmed by Program code 63. And, any station can make a call to the door-phone, which establishes a monitoring.

If door-phone call is not answered within 10 seconds, the system will release the door-phone and stop ringing.

SAMSUNG ELECTRONICS provides the proprietary door-phone and other door-phone may not operate with the system.

Related Control : Connecting Door Phone and Lock Control
Program code 63 (Door Phone Ring Station)

EXTERNAL CALL FORWARD

Incoming call through the assigned outside line (Program code 75) may be automatically transferred to any free CO line when not answered within Transfer Recall Time (Program code 53). And, the digits stored in speed dial entry 99 will be automatically dialed. In this case, the system will not restrict any TOLL. The external call forward duration can be adjusted by Program code 75. This is useful when telephone company call forward is not available.

[illegible]

FAX COMPATIBILITY

By connecting the FAX machine to any single line station port there is no need for a dedicated FAX line. Incoming calls can be transferred to the FAX machine or any outside line can be assigned to FAX incoming by user-programming (Program code 61, 62). Any outside line in the system may be selected to send a FAX.

Related Control : Program Codes related to trunks

FAX DIRECT TRANSFER

By connecting the FAX machine to any single line station port there is no need to remember the FAX station number to transfer. The keyset has the feature button to select FAX station and any single line telephone station can be assigned to FAX station (Program 84). This feature is prepared to transfer a incoming call to FAX station directly when you receive the call at the keyset. Two stations can be assigned to FAX stations at maximum.

Related Control : Program Code 84 (Fax Station Assignment)

FUNCTION ID

The system provides so many features which can not be all served with one-touch access. Therefore, the features which are not designated in keyset buttons may be served with the specific FUNCTION ID after pressing FUNC/DND button. At the single line telephone, all of the features are served as above and its HOOK FLASH means FUNCTION start. All of function ID starts from digit 1.

Related Control : User's Guide

HEARING AID COMPATIBILITY

AS-11 Series are fully hearing aid compatible as specified in FCC Rules and Regulations, Part 68.

LCD DISPLAY (LIQUID CRYSTAL DISPLAY)

Keyset of which suffix is E or EV has a one-line, sixteen (16) character LCD display of which character consists of five (5) by seven (7) dot matrix. Time data, call progressive information, and programming information are shown. The brightness of LCD may be adjusted by slide volume in the right side of keyset.

LOUD BELL

In a noisy place or warehouse, it is very difficult to hear ring tone. An external speaker with AMP may be installed with keyset and ring tone (Incoming thru trunk or Intercom) will be served. A small speaker with AMP is recommended.

Related Control : External Individual Paging Connections
 Program Code 36 (External Individual Paging)

MUSIC SERVICE

MUSIC ON HOLD A held trunk or subscriber may be served with music. In that case, the music is called as Music-On-Hold (MOH).

BACKGROUND MUSIC A subscriber may enjoy the music through his/her telephone. In that case, the music is called as Background Music (BGM).

The system has a Internal music source (Melody chip) and External music interface, which is selected by moving the related shunt pin. The selection effects on all of the system. The selected music source operates as Music-On-Hold or Background Music. If the customer prefers to enjoy silence select the External music source without connection.

Related Control : External Music Source Connections

PAGE, EXTERNAL

A voice pair with 600 ohm impedance is provided for connection to a customer-provided paging system. Any subscriber may make a external page with the connection. The paging capacity is up to the customer paging system and the volume may be adjusted in the external paging system.

PAGE, INTERNAL

Any subscriber can make an internal page through the speakers of keysets, which is accomplished with the system network. Any keyset may be assigned to one of four internal page zones (from zone 1 to zone 4) by user-programming (Program code 34). In addition to these, paging to all keysets can be served, which is zone 0. Any subscriber (keyset or single line telephone) may page the keyset speakers in any zone using the corresponding access code, from zone 0 to zone 4.

Any station may be allowed or denied to try a page by user-programming (Program code 32) and any keyset may be allowed or denied to receive an internal page by user-programming (Program code 33).

Related Control : Program Code 32 (Internal Paging)
 Program Code 33 (Paging Included Station Assignment)
 Program Code 34 (Paging Zone Assignment)

POWER FAILURE TRANSFER

When power to the system is interrupted, outside lines are automatically switched to the designated single line telephones. The system transfers two (2) outside lines to the related single line telephones automatically.

1st outside line	station 7
2nd outside line	station 8

FAX machine is recommended to be connected to one of the above three stations, to use continuously regardless of power failure.

Note that the related station should be used for single line telephone and the related shunt pins should be selected correctly to be served. Refer to the installation manual.

REAL TIME CLOCK

Basic KSU is equipped with a Real Time Clock chip (MSM6242RS) and serves the current time display, system/station alarm service based on it.

Real Time Clock continues its operation regardless of Power Failure, when the Memory Backup Switch "BACK-UP" is selected to ON.

New Date and Time data may be entered by User-programming, Program code 55, and the display format may be selected to 12 Hour mode or 24 Hour mode by User-programming, Program code 27.

Related Control : Memory Backup Switch "BACK-UP" in Base Board
 Program code 55 (Date and Time)
 Program code 27 (Time Display Mode)

R I N G S I G N A L

The system provides ringing voltage required for single line phones. And, keyset has its four kind ring frequencies which can be selected individually.

You may know what type of call you are receiving by the sound of ring signal; c.o. line ring, station ring, and door-phone ring.

Each line and door-phone can be individually programmed to ring up to eight (8) selected stations and can be individually selected to ringing mode.

Related Control : Selecting Ring Frequency in User's Guide
 Program Code 60 (Trunk Ring Mode)
 Program Code 61 (Night Ring Station)
 Program Code 62 (Day Ring Station)
 Program Code 63 (Door Phone Ring Station)

SPEED DIAL. STATION

Allows twenty (20) numbers to be stored in memory for use by dialing two digit speed code. These speed numbers are on a station basis and are used only in the station. Each station may have its twenty (20) individual speed numbers. A maximum of thirty two (32) digits may be stored in each speed dial number. Station speed code starts from 00 to 19. In any speed number three (3) second pause, pulse to tone changeover may be entered. Keypad speed dial can be stored in each keypad by station user-programming (Program code 17). And, speed dial numbers for single line telephones can be stored by user-programming (Program code 35).

You can make a speed dial with function ID 16 or using "SD" buttons.

Related Control : Programming Personal Speed Dial Numbers in User's Guide
Program code 17

um Code 35 (Single Line Telephone Speed Dial Numbers)

SPEED DIAL, SYSTEM

Allows eighty (80) numbers to be stored in memory for use by dialing two digit speed code in any station. A maximum of thirty two (32) digits may be stored in each speed dial number. Speed code starts from 20 to 99 and the last number, speed code 99, may be used for CO-CO connection (External call forward). In any speed number three (3) second pause, pulse to tone changeover may be entered.

You can make a speed dial with function ID 16.

Related Control :

- Program Code 41 (System Speed Dial Numbers)
- Program Code 75 (CO to CO Call Time & Line Selection)
- Setting to Forward Calls in User's Guide

PROGRAMMABLE TIMERS

The system allows user-programming to adjust the following timer values; Hold Recall, Transfer Recall, Flash Time, CO to CO call duration, Door Contact Timer, Ring Detection Time, Dial Start Time, and Alarm duration.

Related Control : Program Code 50 (C.O. Flash Timing)
 Program Code 51 (PBX Flash Timing)
 Program Code 52 (Hold Recall Time)
 Program Code 53 (Transfer Recall Time)
 Program Code 54 (Alarm Time Duration)
 Program Code 56 (Ring Detection Time & Dial Start Time)
 Program Code 59 (Inter-Digit Time and Door Open Time)
 Program Code 65 (Auto Timer)
 Program Code 75 (External Call Forward Time & Line Select)

TOLL RESTRICTION

All of stations may be classified from class A to class F (six classes). Based on its class, the station may be restricted to make a Toll according to the related Allow/Deny table. Class A station has no restriction and class F can make an intercom call only. To assign the class and to adjust the restriction entry may be accomplished by user-programming (Program code 30, 72). Toll restriction effects only on the outside line which is assigned to CO. The outside lines assigned to PBX or the exclusive lines will not be restricted. External call forward is not restricted, too.

Related Control : Program Code 30 (Class of Service)
 Program Code 72 (Deny/Allow codes for class B, C, D, E)
 Program Code 43 (CO or PBX line)

TONE

Call-progressive Tones. Audio indications are provided from Exchange, Central Office, PABX, and Key Telephone System. A subscriber may hear the supplied tones and perceive its status. Generally, dial tone, busy tone, ringback tone, and error tone may be served. SKP - 308H system has a dual-tone generator and provides Dial tone, Busy tone, Ringback tone, Transfer tone, Error tone, Confirm tone, and Burst tone.

VOICE MESSAGE SERVICE

Keyset of which suffix is BV or EV provides sixty (60) minute Voice Message Service. Voice Message Service is divided to Voice Alarm Service and Voice Message Sending service.

Voice Alarm service is divided to three (3) parts. Each voice alarm message can be recorded up to eight (8) seconds. A subscriber can record the maximum three (3) different message and reserve their reproducing time. Then, at the assigned time he can hear the message automatically.

Voice Message Sending service is divided to two (2) parts. One is for the intercom message and the other for outside line. Intercom message can be recorded up to sixteen (16) seconds and outside message can be recorded up to twenty (20) seconds. These are automatically sent to a caller when they are enabled. A subscriber can use this feature for a brief memo message when he is out of office. The outside message may be sent only in the Attendant station to the specific line which is selected by user-programming (Program code 77) Recording the voice message can be accessible in one minute after the related keyset starts to operate.

Related Control : Programming Alarm & Recording Voice Message in User's Guide
 Program Code 16 (Voice Message Service in User's Guide)
 Program Code 77 (Voice Message Sending Trunk Assignment)
 Program Code 70 (Attendant Assignment)

VOLUME CONTROL

Keyset subscriber may adjust the volume of handset receiving, speaker-phone receiving, and ring tone.

Handset receiving volume may be adjusted up to four (4) steps by pressing the volume up/down buttons in using handset.

Speaker-phone receiving volume may be adjusted up to eight (8) steps by pressing the volume up/down buttons in using speaker-phone facility.

Ring tone volume may be adjusted up to eight (8) steps by pressing volume up/down buttons in ringing or by station user-programming (Program code 13).

Although three kind volume can be controlled by pressing the same volume up/down buttons, each volume is handled independently.

Related Control : Program Code 13 (Selecting Ring Frequency in User's Guide)

USER PROGRAMMING

The system may be programmed at any keyset with display. Multiple keysets may be programmed at the same time. User-programming is divided to System and Station user-programming of which access code is composed of two digits. Station user-program codes start from digit 1 and password may not be required, and the data effects only on the keyset.

System user-program codes start from 20 and user password should be known. Otherwise, anyone can not contact to System User-programming. System user-program effects on all of the system.

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ASSEMBLY & DISASSEMBLY

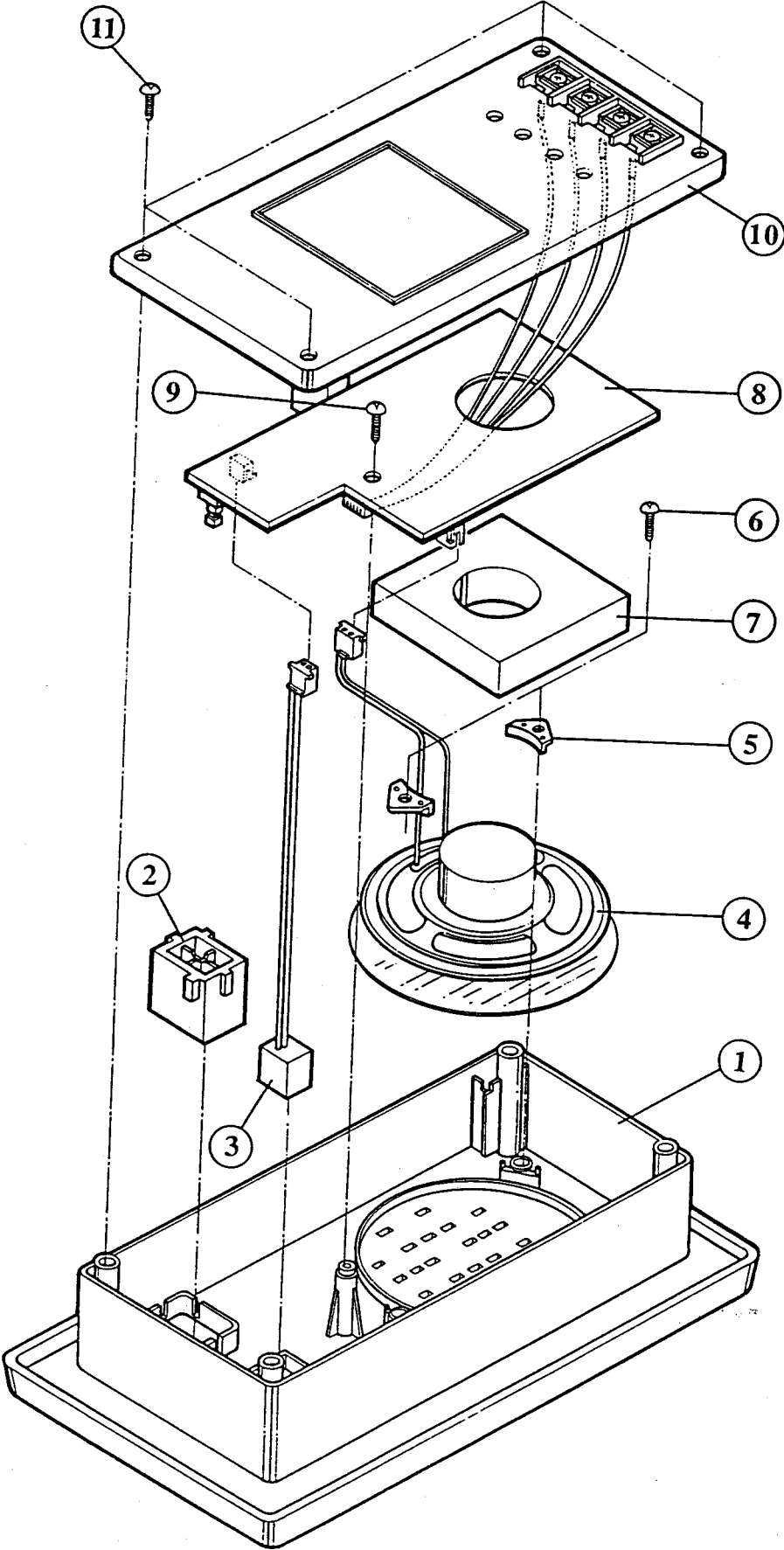
Note that the number marked at the exploded figure indicates the procedure of assembly.

2 . BASIC KSU MECHANICAL PARTLIST

NOTE: FFR-Forecasting Failure Rate per system

NO	PARTS NAME	SEC CODE	Q'TY/SET	FFR
1	BASE HOUSING	821-240108AA	1	.001
2	BRACKET-COMPONENT	813-240201AA	1	.001
3	FUSE HOLDER		1	
4	FUSE-GLASS TUBE		1	
5	SWITCH-ROCKER		1	
6	BATT. MATE-N-LOK ASS'Y		1	
7	MAGNET-CORE		1	
8	POWER SUPPLY CORD		1	
9	TRANSFOMMER		1	
10	MACHINE, A, PH, +, M4, L8	841-810001AV	4	.001
11	SKP-308H, BASE BOARD		1	
12	EARTH CABLE		1	
13	WASHER, M4, 4. 3, 8, T1. 5	855-170004AH	1	.001
14	TAPTITE, B, PH, +, M3, L10	847-501001AC	5	.001
15	FUSE-GLASS TUBE		1	
16	SKP-308H, POWER BOARD		1	
17	WASHER, M4, 4. 3, 8, T1. 5	855-170004AH	1	.001
18	TAPTITE, B, PH, +, M3, L10	847-501001AC	4	.001
19	CABLE		1	
20	ACCESSORY-DUST COVER	821-240003AG	1	.001
21	SIDE COVER	821-240109AA	1	.001
22	TOP-HOUSING	821-240107AA	1	.001
23	MACHINE, A, PH, +, M3, L10	841-810001AC	4	.001
24	HOLE-DUMMY	821-258076CA	4	.001

3. DOOR-PHONE EXPLODED VIEW



4 . DOOR - PHONE MECHANICAL PARTLIST
NOTE: FFR-Forecasting Failure Rate per system

NO	PARTS NAME	SEC CODE	Q'TY/SET	FFR
1	COVER	821-350120AA	1	.001
2	BUTTON	821-350116AA	1	.001
3	MIC ASS'Y		1	
4	SPEAKER ASS'Y		1	
5	SPEAKER FIXING BRACKET	813-250013AE	2	.001
6	TAPTITE, B, PH, +, M3, L6	847-501001AA	2	.001
7	FOAM SPEAKER BAFFLE	829-352001AA	1	.001
8	DOOR-PHONE BOARD		1	
9	TAPTITE, F, B, PH, +, M3, L6	847-502001AA	1	.001
10	CABINET ASS'Y		1	.001
11	TAPTITE, B, PH, +, M3, L8	847-501001AB	4	.001

6 . KEYSET MECHANICAL PARTLIST

NOTE: FFR-Forecasting Failure Rate per system

NO	PARTS NAME	SEC CODE	Q'TY/SET	FFR
1	TOP HOUSING	821-240101EB	1	.001
2	KEY TOP "B" (FUNC.)	821-240104AA	3	.001
3	KEY TOP "A" (SPK VOL)	821-240103AA	2	.001
4	KEY TOP "B" (FUNC.)	821-257637BE	4	.001
5	KEY TOP "B" (HOLD)	821-240104AB	1	.001
6	KEY TOP (3X4)	821-256075AC	1	.001
7	KEY TOP "A" (DSS KEY)	821-257637CC	18	.001
8	CONDUCTIVE RUBBER	821-240106BA	1	.001
9	AS-11/30, KEY BOARD		1	
10	TAPTIGHT, B, PH, +, M2, L6	847-500001AA	10	.001
11	SPEAKER ASS'Y		1	
12	TAPTIGHT, B, PH, +, M3, L6	847-501001AA	3	.001
13	HANGER	821-257537AD	1	.001
14	SPRING	813-255013AA	1	.001
15	HANGER HOLDER	813-255028AA	1	.001
16	TAPPING, F, PH, +, 2, M2. 5, L6	842-840002AC	1	.001
17	PLUNGER	821-240102AA	1	.001
18	DISPLAY-LCD, 16DIG, 5X7DOT		1	
19	CON-FLAT CABLE, 14P, 2. 54		1	
20	TAPTIGHT, B, PH, +, M2, L6	847-500001AA	4	.001
21	LCD LENS	821-257633AA	1	.001
22	GUIDE PAPER	829-240004BB	1	.002
23	GUIDE COVER	821-240105BA	1	.001
24	AS-11/30, CONTROL BOARD		1	
25	TAPTIGHT, B, PH, +, M3, L6	847-501001AA	4	.001
26	MIC ASS'Y		1	
27	BOTTOM HOUSING	821-257631AF	1	.001

NO	PARTS NAME	SEC CODE	Q'TY/SET	FFR
28	VR RUBBER FOOT	ME6784-0000	4	.001
29	WALL MOUNTING BRACKET	821-257636AA	1	.001
30	NAME CARD PAPER C	825-119050GC	1	.002
31	NAME CARD PAPER B	825-119050GB	1	.002
32	NAME CARD PAPER A	825-119050GA	1	.002
33	NAME CARD HOLDER	821-256068AA	1	.001
34	LCD CONTRAST LEVER	821-257634AB	1	.001
35	TAPTIGHT, B, PH, +, M3, L10	847-501001AC	4	.001

* H A N D S E T M E C H A N I C A L P A R T L I S T

NO	PARTS NAME	SEC CODE	Q'TY/SET	FFR
1	HANDSET LOWER	821-250314AC	1	.001
2	PAD-SEALING	821-276002AA	1	.001
3	AUDIO-UNIT, 150, -65.5		1	
4	BRACKET-UNIT1	813-255045AA	1	.001
5	TAPPING, PH, +, 2, M3, L8	842-343013AB	1	.001
6	PAD-SEALING	821-276002AA	1	.001
7	AUDIO-UNIT, 160, 98.5		1	
8	BRACKET-UNIT2	813-255045AB	1	.001
9	TAPPING, PH, +, 2, M3, L6	842-343008AB	1	.001
10	TAPPING, PH, +, 2, M3, L8	842-343013AB	1	.001
11	MODULAR JACK ASS'Y		1	
12	HAND SET UPPER	821-250264AC	1	.001
13	TAPPING, PH, +, 2, M3, L8	842-343013AB	1	.001
14	HANDSET CORD		1	

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ELECTRICAL INFORMATION

The contents of this chapter may differ with your system.
SAMSUNG ELECTRONICS may change the system for the improvement
of quality or any reason.

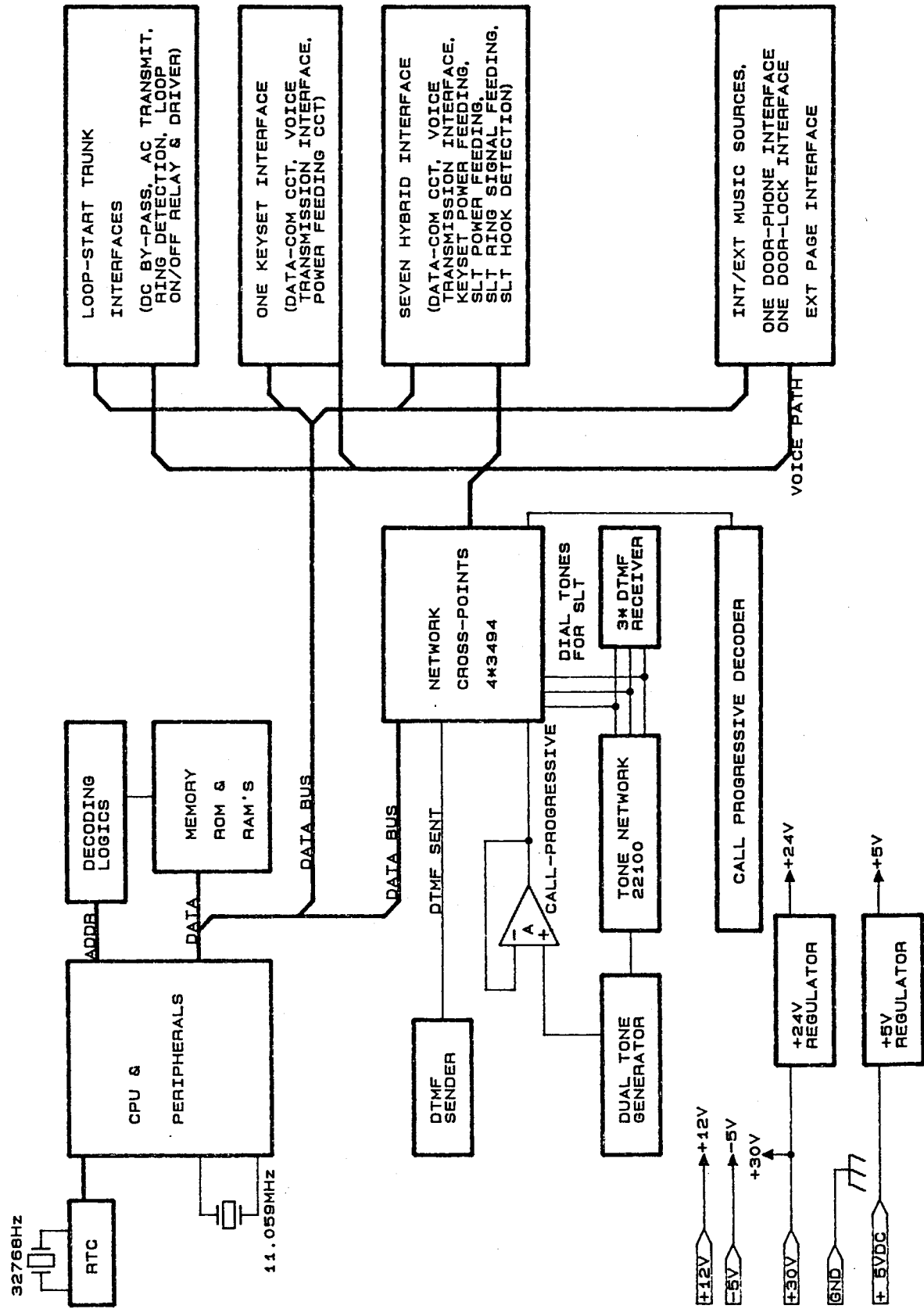
1 . C I R C U I T D E S C R I P T I O N

This section describes the circuit operation of the system and keyset. For easy understanding, the system and keyset circuitry are divided to parts and described in detail after the block diagrams.

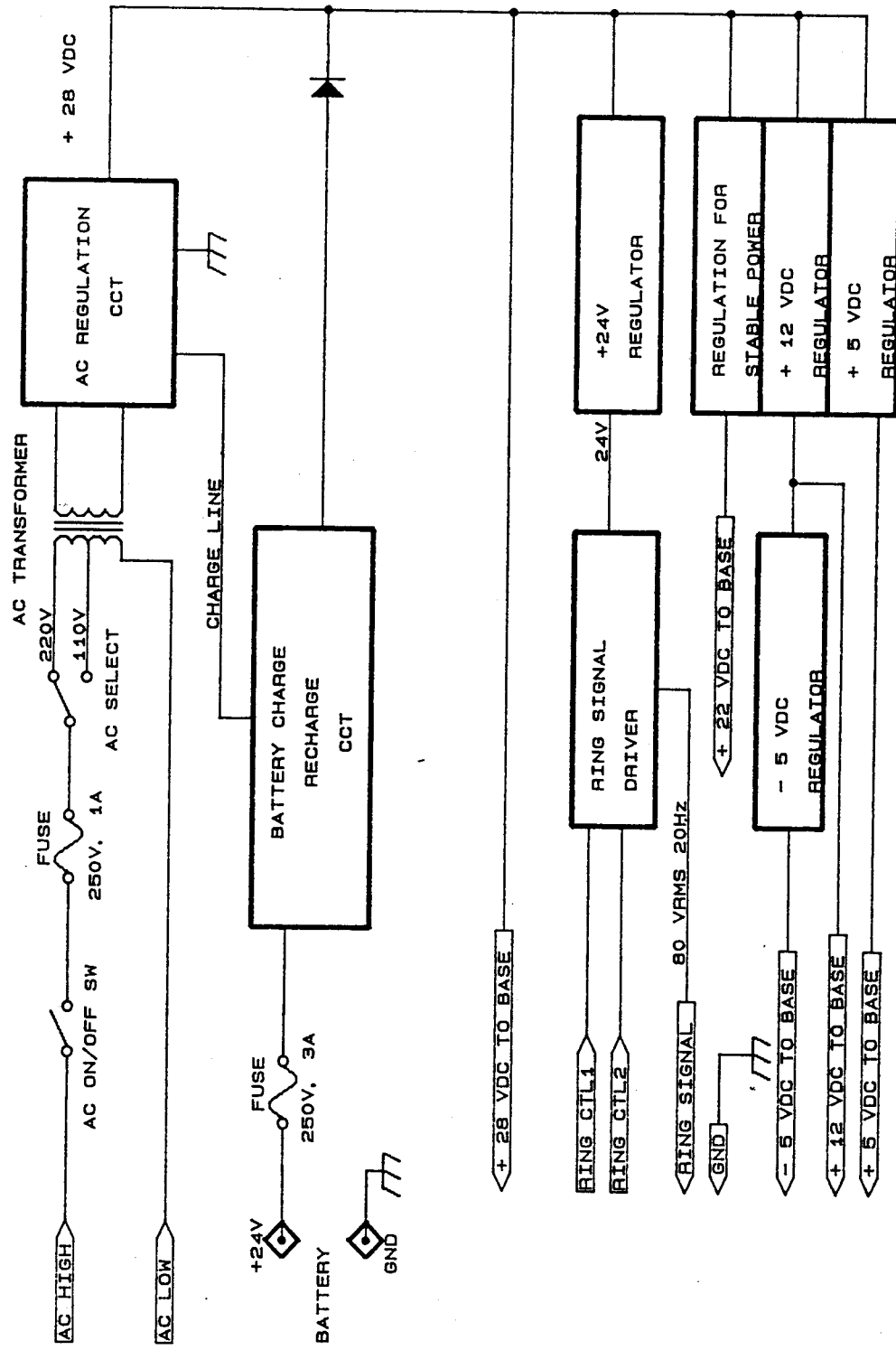
This section is composed of the following contents:

A. System Power B'd Block Diagram	60
B. System Base B'd Block Diagram	61
C. System Control Map	62
D. System Circuit Description	68
E. Door-phone Block Diagram	103
F. Door-phone Circuit Description	104
G. Keyset Block Diagram	105
H. Keyset Control Map	106
I. Keyset Circuit Description	112

B. SYSTEM BASE B'D BLOCK DIAGRAM



A. SYSTEM POWER B'D BLOCK DIAGRAM



C. SYSTEM CONTROL MAP

Address	R/W	Function Description
Program Memory 0000H - 0FFFFH	r	64 Kbyte program memory (27512, EPROM) D0 - D8 : byte access
Data Memory 0000H - 7FFFH	r/w	32 Kbyte data memory (62256, SRAM) D0 - D8 : byte access
8000H	r/w	RTC 1-second digit register access (low state) (MSM6242BRS : U6 pin 2, with A0 - A3) D0 - D3 : 1-second digit data
8001H	r/w	RTC 10-second digit register access (low state) (MSM6242BRS : U6 pin 2, with A0 - A3) D0 - D2 : 10-second digit data
8002H	r/w	RTC 1-minute digit register access (low state) (MSM6242BRS : U6 pin 2, with A0 - A3) D0 - D3 : 1-minute digit data
8003H	r/w	RTC 10-minute digit register access (low state) (MSM6242BRS : U6 pin 2, with A0 - A3) D0 - D2 : 10-minute digit data
8004H	r/w	RTC 1-hour digit register access (low state) (MSM6242BRS : U6 pin 2, with A0 - A3) D0 - D3 : 1-hour digit data
8005H	r/w	RTC pm/am, 10-hour digit register access (low state) (MSM6242BRS : U6 pin 2, with A0 - A3) D2 : pm/am D0 - D1 : 10-hour digit data
8006H	r/w	RTC 1-day digit register access (low state) (MSM6242BRS : U6 pin 2, with A0 - A3) D0 - D3 : 1-day digit data

Address	R/W	Function Description
Data Memory 8007H	r/w	RTC 10-day digit register access (low state) (MSM6242BRS : U6 pin 2, with A0 - A3) D0 - D1 : 10-day digit data
8008H	r/w	RTC 1-month digit register access (low state) (MSM6242BRS : U6 pin 2, with A0 - A3) D0 - D3 : 1-month digit data
8009H	r/w	RTC 10-month digit register access (low state) (MSM6242BRS : U6 pin 2, with A0 - A3) D0 : 10-month digit data
800AH	r/w	RTC 1-year digit register access (low state) (MSM6242BRS : U6 pin 2, with A0 - A3) D0 - D3 : 1-year digit data
800BH	r/w	RTC 10-year digit register access (low state) (MSM6242BRS : U6 pin 2, with A0 - A3) D0 - D3 : 10-year digit data
800CH	r/w	RTC week digit register access (low state) (MSM6242BRS : U6 pin 2, with A0 - A3) D0 - D2 : week digit data
800DH	r/w	RTC control register D access (low state) (MSM6242BRS : U6 pin 2, with A0 - A3) D0 : Hold D1 : Busy D2 : IRQ flag D3 : 30 second adjustment
800EH	r/w	RTC control register E access (low state) (MSM6242BRS : U6 pin 2, with A0 - A3) D0 : Mask D1 : Interrupt/Standard D2 : STD.P period 0 D3 : STD.P period 1

Address	R/W	Function Description
Data Memory 800FH	r/w	RTC control register F access (low state) (MSM6242BRS : U6 pin 2, with A0 - A3) D0 : Reset D1 : Stop D2 : 24/12 D3 : Test
9000H	w	DTMF sender latch enable (falling edge) (74HCT374 : U20 pin 11) D7 D6 D5 D4 D3 D2 D1 D0 H L L L L H H H DTMF 1 H L L L H L H H DTMF 2 H L L L H H L H DTMF 3 L H L L L H H H DTMF 4 L H L L H L H H DTMF 5 L H L L H H L H DTMF 6 L L H L L H H H DTMF 7 L L H L H L H H DTMF 8 L L H L H H L H DTMF 9 L L L H L H H H DTMF * L L L H H L H H DTMF 0 L L L H H H L H DTMF # other states inhibited
0A000H	r	c.o. ring, door call detector and CPD valid, DTMF receiver valid read enable (low state) (74HCT244 : U15 pin 1, 19) D0 : co 1 ring/loop detection, low_detect D1 : co 2 ring/loop detection, low_detect D2 : co 3 ring/loop detection, low_detect D3 : co 4 ring/loop detection, low_detect D4 : 1st DTMF receiver StD, high_detect D5 : 2nd DTMF receiver StD, high_detect D6 : 3rd DTMF receiver StD, high_detect D7 : CDP valid, high_detect
0C000H	r	Keyset data RX buffer latch enable (low state) (74HCT244 : U13 pin 1, 19) D0 : 1st keyset RX data D1 : 2nd keyset RX data (hybrid) D2 : 3rd keyset RX data (hybrid) D3 : 4th keyset RX data (hybrid) D4 : 5th keyset RX data (hybrid) D5 : 6th keyset RX data (hybrid) D6 : 7th keyset RX data (hybrid) D7 : 8th keyset RX data (hybrid)

Address	R/W	Function Description
Data Memory 0D000H	r	CPD data read enable (active_high) (NE5900 : U22 pin 14) D2 D1 D0 (D3 - D7 : reserved) L L L Dial Tone L L H Ringback Tone L H L Busy Tone L H H Reorder Tone H H H Overflow other states Invalid
0E000H	r	Hybrid port SLT hook detect buffer read enable (low state) (74HCT244 : U16 pin 1, 19) D0 : reserved D1 : 2nd station SLT hook detection, low_det D2 : 3th station SLT hook detection, low_det D3 : 4th station SLT hook detection, low_det D4 : 5th station SLT hook detection, low_det D5 : 6th station SLT hook detection, low_det D6 : 7th station SLT hook detection, low_det D7 : 8th station SLT hook detection, low_det
0F000H	w	CPD clear, Doorphone on, Ring signal on (active_high) (74HCT374 : U19) D3 : H : Doorphone ON : pin 9 D4 : H : CPD clear : pin 12 D5 : H : Ring signal ON : pin 15
0F001H	w	Network control data latch enable (falling edge) (74HCT374 : U8 pin 11) D0 : on/off control data, high_active & tone network row address 0 D1 : network row address 0 tone network row address 1 D2 : network row address 1 tone network column address 0 D3 : network row address 2 tone network column address 1 D4 : network row address 3 tone network on/off control, high_active D5 : network column address 0 D6 : network column address 1 D7 : network column address 2 co-operated with port 1.0

Address	R/W	Function Description
Data Memory 0F003H	w	SLT Relay driver (hybrid port) latch enable (high state) (UCN5801A : U18 pin 2) D0 : reserved D1 : station 2 SLT relay control, high_active D2 : station 3 SLT relay control, high_active D3 : station 4 SLT relay control, high_active D4 : station 5 SLT relay control, high_active D5 : station 6 SLT relay control, high_active D6 : station 5 SLT relay control, high_active D7 : station 6 SLT relay control, high_active
0F004H	w	Keyset data TX buffer latch enable (falling edge) (74HCT374 : U12 pin 11) D7 : 1st keyset TX data D6 : 2nd keyset TX data (hybrid) D5 : 3rd keyset TX data (hybrid) D4 : 4th keyset TX data (hybrid) D3 : 5th keyset TX data (hybrid) D2 : 6th keyset TX data (hybrid) D1 : 7th keyset TX data (hybrid) D0 : 8th keyset Tx data (hybrid)
0F005H	r	1st DTMF receiver output enable (high state) (MT8870C : U23 pin 10) Refer to following
0F006H	r	2nd DTMF receiver output enable (high state) (MT8870C : U24 pin 10) Refer to following
0F007H	r	3rd DTMF receiver output enable (high state) (MT8870C : U25 pin 10) D3 D2 D1 D0 (D4 - D7 : reserved) L L L H DTMF 1 L L H L DTMF 2 L L H H DTMF 3 L H L L DTMF 4 L H L H DTMF 5 L H H L DTMF 6 L H H H DTMF 7 H L L L DTMF 8 H L L H DTMF 9 H L H L DTMF 0 H L H H DTMF * H H L L DTMF #

Address	R/W	Function Description
Data Memory 0F00AH	w	c.o. loop, door lock relay driver latch enable (high-state) (UCN5801A : U1735 pin 2) D0 : c.o. 1 loop relay control, high_active D1 : c.o. 2 loop relay control, high_active D2 : c.o. 3 loop relay control, high_active D3 : reserved D4 : Door Lock relay control, high_active D5 - D7 : reserved
Port Control		
P1.0	w	network strobe (high state) (M3494 : U27 pin 18) co-operated with control 0F001H.
P1.1	w	Tone network strobe (high state) (CD22100 : U9 pin 7) co-operated with control 0F001H.
P1.2 - P1.6		reserved
P1.7	w	Watch-dog strobe (DS1232 U48 pin 7)
P3.0 - P3.5		reserved
P3.6	w	RD : read signal
P3.7	w	WR : write signal

D. SYSTEM CIRCUIT DESCRIPTION

This section includes the following circuit descriptions:

Power Supply Board

- AC/DC Converter
- System Back-up Interface
- Ring signal Generator
- Power Regulator

Base Board

- CPU & Control Logics
- Real Time Clock
- Memory Backup circuit
- Network
- Tone generator & Tone network
- CPD
- DTMF Sender
- DTMF Receivers
- Trunk interfaces
- Keyset interfaces
- SLT interfaces
- Music sources
- Door-phone interfaces
- External Page interface
- Power Regulator

Refer to the related circuit diagrams in the section 3 for easy understanding.

POWER SUPPLY BOARD

This board provides the main DC power for all of the system operation. In addition, system back-up interface and ring signal generator are also equipped.

AC/DC CONVERTER

The system is equipped with AC-to-DC power supply for its operation. 110 VAC or 220 VAC are allowable of which frequency is 50 Hz or 60 Hz. The input power may be selected with the selection switch. And, the system has a ON/OFF control switch for connecting or dis-connecting the input power to the system.

AC input is composed of three terminal; AC high, AC low, and Earth terminal. The earth terminal is provided from the local electric company or the electric transmission pole, which is used for the protection circuitry. To ground the system is very important for system protection from any damage, so the system provides the additional earth plug where the earth terminal of AC power is not sured.

The AC power through the ON/OFF control switch is fed to the AC power fuse and the protection circuitry. The fuse capacity is 1 A, 250 V and it protects from the input over-voltage and the output shortage. And, the protection circuitry is composed of a varistor, which enhance the system noise and surge blocking. The varistor is applied differently as the input voltage; 470 V varistor for 220 VAC and 220 V varistor for 110 Vac. The varistor is parallel connected between AC high and AC low terminal for the normal mode protection. Any over-voltage input is clipped to the level of the varistor and the fuse may operate to blow at that case. Another 470V varistor is installed between AC low and the earth for the common mode protection of which clipping level is 470 volt. Any over 470 V input in common mode will be clipped to the level of varistar. As above, the circuitry protects the system from any over voltage of the AC power input.

The power through the protection circuitry is fed to the power transformer. The power transformer isolates the output from the input and provides the the output according to the turn ratio. The primary turn is center-tapped for the reception of the input based on the power level. Full turn is for 220 VAC input and the center-tapped terminal is connected to 110 VAC input. The secondary turn is separated to two part; one for the main power source and the other for charging the external battery. The output of the main secondary turn is also a sine wave, which is fully rectified by the following bridge diode. The rectified wave is regulated by the large capacitance capacitor (4700 uF/50 V, C1). With the capacitor, the waveform is as DC and the regulation is some different as the load variation, which has a little power signal as a ripple. Therefore, the output is regulated again at the next circuitry.

SYSTEM BACK-UP INTERFACE

The system may continue the full system operation during AC power failure or "brown-outs" when a 24V battery supply is connected. At the Power Supply board charging and discharging circuits are prepared for the external battery. The system back-up interface is composed of battery charge circuit, battery discharge circuit, and protection circuit.

Battery charge circuit is for charging the battery while AC power fed. At first, a switch is prepared to control the path of charging. The path switch is composed of a transistor (TIP42C, Q2) and resistor R1 (1.8K). If the transistor turns ON, the external battery can be charged. Otherwise, charging process may be blocked owing to the large resistance of R1.

A low level input to the transistor base can turn it ON because the transistor is a PNP type. The transistor can be driven by the comparator, LM393 (U4A). The driving point may be decided as following:

The inverting terminal is provided with a reference voltage, 6.2 volt of zener voltage (1N4735A, ZD1). And, the input is fed to the non-inverting terminal, which is provided from the battery through a signal diode, some resistors, and a variable resistor. With the structure of the circuit, you may get the detected level.

$$\text{Detected level} = (VR1 + R7 + R6 + R9)/R9 * 6.2V + 1.0V$$

The above equation says that the detected level may be varied according to the resistance of the variable resistor. The calculated output is 28.8V at maximum and 26.2V at minimum.

The transistor can be driven by the comparator of which the detected value is as above. In factory, it is recommended to adjust the level to 28.0V. Therefore, the charging path is still connected until the battery level is up to 28.0V and the path may be dis-connected when the battery level is over 28.0V, which protects the battery from over-charge. It is usually called as Over-Charge Protection circuit.

After the over-charge protection switch a posistor is connected serially, which prevents over-current flow while charging because any over-current may interfere the main DC to fall and it may activates system restart. The restricted current flow at the posistor is 320 mA and its trip current is 710 mA. The device may endure 30 seconds at the maximum current flow, 1.4 A. (PTH63AR6R8M2B491, PSW2). The rectifier diode, 1N4004, D6 prevents any reverse current flow while discharging or AC power failure.

Battery discharge circuit consists of rectifier diode. The rectifier diode, 1N5401, D1 prevents any reverse current flow while there is no reason to discharge from the battery. The rectifier diode has larger capacity, 3A than 1N4004, 1A.

The comparator output is determined by the input level. The non-inverting terminal is provided with the reference voltage by a zener diode (ZD1) and two signal diodes (D4 and D5). The zener diode provides 6.2V zener voltage and the signal diodes provide the hysteresis. Owing to the signal diodes, the reference level varies to 5.75V or 6.65V according to the comparator output. The additional comparing circuit with LM393, U9B provides a driving current for the signal diodes.

The inverting terminal is provided with the battery voltage, which is adjusted to a adequate level divided by some resistors. The detection level may be known as following:

$$\begin{aligned}\text{High Detected Level} &= (VR1 + R7 + R6 + R9)/(R6 + R9) * 6.65 + 1.1 \\ &= 24.6 \text{ volt}\end{aligned}$$

$$\begin{aligned}\text{Low Detected Level} &= (VR1 + R7 + R6 + R9)/(R6 + R9) * 5.75 + 1 \\ &= 21.4 \text{ volt}\end{aligned}$$

At the above equation, the resistance of the variable resistor has one value because the value is already set while adjusting the over-charge protection level.

The battery can be connected via its prepared connector and harness ass'y. The black lead should be connected to the low potential of the battery and the red lead should be connected to the high potential of the battery.

RED lead	-	Plus
BLACK lead	-	Minus

For protecting the battery from over-load and the reverse connection, 3A capacity fuse is connected serially. It is equipped at the power supply board and you may replace with same capacity fuse if necessary. When the leads are reversely connected, the rectifier diode D1 will be activated and the fuse will blow.

Be cautious to install the live battery. The battery may have the sufficient energy to damage the system or to injure a person. After connecting the related leads of the harness to the battery, you should install the battery to the system during the system operation. Otherwise, the discharging current may exceed too much to injure you.

RING SIGNAL GENERATOR

Ring signal is provided to single line telephones for on-hook signalling which indicates a call. The system provides 80Vrms, 20Hz, and pulse signal for ring.

Ring signal generator have two parts, 80VDC generation part and 20 Hz signal generation part.

To make 80 VDC, 5 KHz AC signal from NE556 (U1A) is applied to Q6, Q7 via transformer 5692 (T1).

ON/OFF signal of Q6 and Q7 which is corresponded to 5 KHz signal is applied to primary turn of ST-1AB supplied 21V power. And then, the secondary turn of ST-1AB generate high voltage AC signal.

This high voltage signal is rectified by Bridge diode (BD4) and C25 (100uF/100V) and turn to be DC 80 V power.

With another NE555 (U1B), 20 Hz AC signal is generated and alternate the DC 80 V power with photo TR PC827 (U2, U3). Therefore we can get AC 80 Vrms 20 Hz Ring signal.

And this Ring signal is generated when the SLT port need ring signal by the control of TR (Q4, Q5) to which bases are connected to R/C port (74HCT374 U19 pin 15). The generated ring signal is transfered to the necessary SLT ports.

For a reference, the technology of power supply is largely divided to two; Linear regulator and Switching regulator.

The linear regulator has a low efficiency and noise and the switching regulator has a high efficiency and noise. And, the switching regulator is more expensive than the linear. We usually use two technology mixed.

The switching regulators are used for high-consumed power and the linear regulators are used for low-consumed power. To design and apply the switching regulators needs the high notice to reduce the noise.

POWER REGULATOR

At the power supply board, the common-used and low-consumed powers are regulate and provided to each parts; Regulated DC, +12V, -12V, and -5V. Among them, minus 12V power is not used at any board and it is for the regulation of minus five volt power.

Regulated DC is provided for power feeding to single line telephones.

The main DC from power supply board can not be used owing to the ripple which results in the hum noise.

A simple linear technique is used for regulation. The transistor Q12 and Q13 are composed for darlington circuit to improve the gain and to decrease the loss, which are the pass element of the linear regulator. The zener diode ZD3 provides a reference voltage and the resistors R31 give the feedback to control the pass element.

The output voltage may vary from 21.5 volt to 23.0 volt according to the zener tolerance.

Generally, as already described, a linear regulator has a low efficiency and low noise output. But the linear regulator as this has a good efficiency owing to the small drop between the input and the output.

In the regulation circuit, the largest factor to decrease the efficiency is the performance of pass element, and the pass element is composed with darlington circuit to increase the gain, which enhances the performance and reduces the loss.

Plus 12 volt regulator uses the linear technology and all the necessary circuitry is combined to one chip 7812, which is supplied by some semiconductor manufactures. For small power-consumed system, the linear technology is popular owing to the low price and the simple application circuit with the related chip. Only the input and output capacitors are necessary for the additional devices. In addition, a small capacitance capacitor may be available because of the minute noise. The system uses the larger capacitance device for more stability but it is the designer's groundless apprehensions. For the plus 12 volt regulator, the main DC from power supply board is fed. The electrical characteristics of 7812CT are as follows:

Maximum Input Voltage	35V
Output Voltage	11.4V min, 12.0V typ, 12.6V max
Line Regulation	13mV typ, 240mV max
Load Regulation	46mV typ, 240mV max
Quiescent Current	4.4mA typ, 8.0mA max
Ripple Rejection	60dB typical
Dropout Voltage	2.0V typical
Output Resistance, 1KHz	18m Ω
Short Circuit Current Limit	0.2A typical
Peak Output Current	2.2A typical
Temperature factor of output	- 1.0mV/°C

Plus 12 volt is mainly used for sending data to keysets and providing the power to door-phones.

Minus 12 volt regulator uses the switching technology. Linear technology can not support inverting or step-up regulator, and the minus 12 volt regulator needs the inverting process from the plus 12 volt power. The main part of the regulator is PWM device and 78S40 is used. PWM is a abbreviation for Pulse Width Modulation which generates the pulse signal for switching.

For the pass control, the transisitor TIP42C, Q15 is equipped and the inverting process is accomplished with the inductor and the high speed diode. The output of the regulator, minus 12 volt, is provided to each board but is not used at any board owing to the lapse of memory. In the current system, the output is used only for the minus 5 volt regulator input.

The electrical characteristics of 78S40 are as follows:

Maximum Input Voltage	40V
Reverse-Power Diode Voltage	40V max
Current through Power Switch	1.5A max
Current through Power Diode	1.5A max
Reference Voltage	1.18V min, 1.245V typ, 1.31V max
Reference Voltage Line Regulation	0.04mV/V typ, 0.2mV/V max
Reference Voltage Load Regulation	0.2mV/mA typ, 0.5mV/mA max
Oscillator Charging Current	20uA min, 70uA max
Oscillator Discharge Current	150uA min, 350uA max
Oscillator Voltage Swing	0.5V typical
Current Limit Sense Voltage	250mV min, 350mV max
Output Transistor Current Gain	70 typical
Output Leakage Current	10nA typical
Output Source Current	75mA min, 150mA typ
Output Sink Current	10mA min, 35mA typ
Output Low Voltage	1.0V maximum
Output High Voltage	(VCC - 3.0V) minimum

Minus 5 volt regulator is composed of the linear regulation chip, 7905, which pulls minus 12 volt down to minus 5 volt. It is a Integrated Chip provided by so many semiconductor manufacturers. Owing to the linear technology, the regulated output has little ripple noise and its efficiency is low. But, minus 5 volt's power coconsumption is a little and its composition is very simple, then the regulator is composed with the linear technology. The electrical characteristics of 7905CT are as follows:

Input Voltage	- 35V max
Output Voltage	- 4.8V min, - 5.0 typ, - 5.2 max
Line Regulation	35mV typ, 100mV max
Load Regulation	11mV typ, 100mV max
Input Bias Current	4.3mA typ, 8.0mA max
Output Noise Voltage	40uV typical
Ripple Rejection	70dB typical
Temperature factor of output	- 1.0mV/°C typical

Minus 5 volt is mainly used for the amplification and transmission of the audio signals, which provides the low potential compared that plus 5 volt regulated at each board provides the high potential.

Plus 5 volt regulator used the switching mode power supply, SI8301L. IT's specifications are as follows.

Input Voltage	45V ma
Output Voltage	4.9V min, 5V typ, 5.1V max
Output Current	1A max
Efficiencyen	60% min

The regulator does not have any short protection circuit and the thermistor is applied to the input serially.

BASE BOARD

This is the main printed circuit board that contains CPU, memory, common control, and switching circuitry. It provides interfaces for telephone lines 1 through 3 which are the subscriber lines from the central office or PBX, stations 1 through 8, and the additional features; music on hold & background music sources, external paging interface, power failure transfers for line 1 through line 2, one door-phone with lock release contact and memory backup battery.

For easy understanding, the circuit of base board is divided and described respectively; CPU & Control Logics, Real Time Clock, Memory Backup circuit, Network, Tone generator & Tone network, CPD, DTMF Sender, DTMF Receivers, Trunk interfaces, Keyset interfaces, SLT interfaces, Music sources, Door-phone interfaces, External Page interface, and Power regulator.

CPU & CONTROL LOGICS

CPU and control logics exist in main board and control all of the system operation and features. They are composed of CPU, reset circuitry, memory, and decoders.

SKP-308H system is equipped with 8031 as its CPU (Central Process Unit) which is supplied by Intel. The CPU is one of MCS51 series and has no internal program memory. Its major features are as follows:

- ◆ Eight (8) bit CPU
- ◆ On-chip Oscillator
- ◆ None of Internal Program Memory
- ◆ 128 bytes of Data Memory
- ◆ 21 Special Function Registers
- ◆ 32 I/O lines
- ◆ 64K address space for External Program Memory
- ◆ 64K address space for External Data Memory
- ◆ Two 16-bit Timer/Counters
- ◆ A five-source interrupt structure with two priority levels
- ◆ A full duplex serial port
- ◆ Bit addressability for Boolean processing

The system clock is provided by 11.059MHz crystal, and its machine cycle is 1.085 micro-seconds which results from the system clock divided by 12, because one machine cycle of 8031 CPU is composed of twelve system clocks. For good oscillation without distortion, two by-pass capacitors are attached to the terminals of the crystal.

8031 CPU has the internal oscillator and any additional oscillator may not be required.

CPU operates with plus 5 volt power, system clock, and reset free. You may check the three factors if you have any trouble. It has four ports and each port is composed of eight terminals which are also usually called as ports.

Port 0 is used for 8-bit data bus and the lower 8-bit address. The lower address and data are multiplexed at the port which is shared on time basis. During address latch cycle, the port gives the lower address with the activation of ALE (address latch enable). Therefore, a latch buffer is connected to get and store shortly the address. After address latch, port 0 acts as data bus. The port has a high impedance state and the external pull-up resistors have to be applied; Resistor array RA1. The resistance of pull-up may be determined according to driving capability. The system uses 10 K ohm for this. Port 0 swings from Low to High continuously and at random. If you find one member of port 0 stuck to one level, you may know that one of devices which are connected to port 0 is out of order.

Port 1 is used for driving I/O directly. It has the internal pull-up resistors and there is no need to attach any additional pull-up resistors. The system uses this port for strobe of network, tone network and watch-dog clear signal. The port is activated at the necessary time, high or low, and the duration is too small.

Port 2 is used for the upper address signals. It has the internal pull-up's to drive. Used exclusively, and any additional device may not be needed. Port 2 fluctuates continuously and its period is random. Sticking to one level means the device related to this port may be out of order.

Port 3 has the internal pull-up's to drive and any additional pull-up resistor is not attached. Port 3 consists of eight special ports and each port operates as I/O or the other function. Port 3.6 acts as the read signal, active-low, and port 3.7 as the write signal active-low, too. Reading operation from the data memory activates the port 3. and writing operation to the data memory activates the port 3.7, then the ports are used for read/write enable signals.

PSEN port is for the program fetch and ALE for the address latch of port 0.

The CPU characteristics are as follows:

Ambient Temperature Under Bias	from 0 °C to 70 °C
Storage Temperature	from - 65 °C to 150 °C
Voltage on each pin at maximum	from - 0.5V to 7V
Package Power Dissipation	1.5 W
Operating Power Supply	5V ± 10 %
Input Low Voltage (except EA)	from - 0.5V to 0.8V
Input Low Voltage EA	from VSS to 0.7V
Input High Voltage (except XTAL2, RST, EA)	from 2.0V to VCC + 0.5V
Input High Voltage XTAL2, RST	from 2.5V to VCC + 0.5V
Input High Voltage EA	from 4.5V to 5.5V
Output Low Voltage	0.45V maximum
Output High Voltage	2.4V minimum
Power Supply Current	135 mA max while all outputs dis-connected
Pin Capacitance	10 pF max at 1MHz
Oscillator Frequency	from 3.5 to 12.0MHz
ALE Pulse Width	127 nS min at 12MHz
PSEN Pulse Width	215 nS min at 12MHz
RD Pulse Width	400 nS min at 12MHz
WR Pulse Width	400 nS min at 12MHz

In addition to the above, so many informations are required to design a system but they may be enough to support our system. If you need the more and detail informations, refer to the data book provided by Intel.

8031 has two 16-bit timers internally and any external timer will not be required.

To protect CPU from a electrical shock or trap, a reset circuitry may be needed, which is generally composed of a Level Detector and a Watch-dog circuit. The reset circuitry of the system consists of a micromonitor chip CD1232 U48. CD1232 chip monitors two vital condition for CPU; power supply level variation and watch dog timer.

And, 8031 is equipped with High active reset logics and any input above 2.5 volts will be detected as a reset signal, of which duration should be 2 machine cycles at minimum.

Level Detector detects the variation of CPU power, which is 5 volt for 8031 CPU. It resets CPU and its internal memory for protection, if power is under-range. Intel guarantees 8031 operates well within 10 percents variation of the power.

The Level Detector protects CPU from the power variation, which stabilizes the CPU operation and enhances the system reliability.

A Watch-dog circuit monitors the CPU operation, and resets CPU if an abnormal status is detected, escaping from the unpredicted program trap or circuit trap.

Watch-dog circuit is in the micromonitor chip CD1232. If there is no strobe signal within 100ms at CD1232 U48 pin 7, Reset signal is generated at pin 5. The input trigger of Watch-dog circuit time is 100ms maximum, and reset time is 250ms to 500ms.

Port 1.7 of CPU provides a continuous triggering signal for Watch-dog circuit, and if there is some problem in s/w running, the trigger pulses may be stuck at abnormal status.

The CPU characteristics are as follows:

Operating Temperature	from 0 °C to 70 °C
Storage Temperature	from -40 °C to 85 °C
Operating Power Supply	5V ± 10 %
Input Low Voltage (ST)	from - 0.3V to 0.8V
Input High Voltage (ST)	from 2.0V to VCC + 0.3V
Power Supply Current	2 mA max
Pin Capacitance	5 -7 pF
RESET active Time	250 ms to 500 ms
ST Pulse Width	10 nS min

The system memory is divided to Program memory and Data memory. 64Kbyte EPROM (Erasable & Programmable Read Only Memory, 27512) is used for the system program memory. And, 32Kbyte SRAM (Static Random Access Memory, 62256) is used for the system data memory.

~~Program memory has all instructions for system operations, and the contents are stored in factory, which any user can not approach.~~

CPU (8031) reads the instruction at each machine cycle and acts as the instruction commands, which is usually called as program fetch cycle. And, port 0 of CPU is multiplexed with low byte of program address and data.

Therefore, the address latch enable (ALE) signal is activated whenever the instruction is read. For the address latch, a latch device (74HCT373, U2) is prepared.

The PSEN (U1 pin29) signal is connected to the output enable of EPROM, which enables to read the instruction via data bus (Port 0). At the program fetch cycle, any read or write signal (U1 pin 17 or pin 16) may not be activated. CPU reads the program on byte basis.

~~Data memory has all data to control and to be programmed by users.~~ To make a access to the data memory, a bi-directional buffer is used for data bus. This buffered data bus is connected to the devices for reading the data or driving. Data memory may be protected when power failure with the memory backup circuit of which operation will be described later.

The data memory's characteristics are as following:

Operating Voltage Range	from 4.5V to 5.5V
Input High Voltage	from 2.2V to VCC + 0.3V
Input Low Voltage	from - 0.3V to 0.8V
Output High Voltage	2.4V minimum
Output Low Voltage	0.4V maximum
Input Capacitance	10 pF maximum
Standby Current (VCC = 2.0 to 5.5V)	2 uA typ, 100 uA max

The first 32Kbyte block of data memory address is allocated to data memory, and the last 32Kbyte block is allocated to I/O controls.

I/O controls may be activated only when the MSB (A15) is high and the control signals is divided by some decoders. The first decoder is 74HCT154, U10 and The second decoder is 74HCT138 U11.

74HCT154 (U10) is a four to sixteen decoder and A12 to A15 are fed to the inputs, which are decoded to one of sixteen outputs. The first output to the eighth output can not be used because the block is duplicate to data memory. Chip selection can be accomplished with enabling read signal or write signal which is the output of 74HCT08 (U30C).

A15	A14	A13	A12	Function
L	X	X	X	Data Memory Block
H	L	L	L	RTC Chip Select 0
H	L	L	H	DTMF Sender Latch Enable
H	L	H	L	DTMF Receiver Valid, CPD Valid, C.O ring detect Door Call Detect.
H	L	H	H	Reserved
H	H	L	L	Keyset Data RX Buffer latch Enable
H	H	L	H	CPD Data Read Enable
H	H	H	L	Hybrid Port SLT Hook Detect Buffer Read Enable
H	H	H	H	2nd Decoder 74HCT138 U11 Select

74HCT138 (U11) is a three to eight decoder of which inputs are provided A8 to A10 and one of the first decoder outputs.

A15	A14	A13	A12	[1111B] determined by the first decoder
A2	A1	A0		Function
L	L	L		CPD clear, Doorphone ON, Ring Signal ON
L	L	H		Network Control Data Latch Enable
L	H	L		C.O Loop, Door Lock Relay Driver Latch Enable (with A3 = 1 state)
L	H	H		SLT Relay Driver Latch Enable
H	L	L		Keypad Data TX Buffer Latch Enable
H	L	H		1st DTMF Receiver Output Enable
H	H	L		2nd DTMF Receiver Output Enable
H	H	H		3rd DTMF Receiver Output Enable

All of I/O controls for main board are determined with the above two decoders.
Refer to system control map for detail.

In addition, ports of CPU control directly some devices. Port 1.0 send the strobe signal to network chip in main board. The strobe signal is active high and the latched data at the related buffer selects a cross-point and controls the switch ON/OFF. Port 1.1 send the strobe signal to tone network chips in main board. The strobe signal is also active high and the latched data controls the cross-point.

Port 1.7 is assigned to the clock signal of Watch-dog circuit and port 3.6 and port 3.7 are assigned to the RAM Access control.

REAL TIME CLOCK

The system is equipped with a real time clock, MSM6242BRS, which provides the precise timebase for the current time. It has an on-chip oscillator for 32.768 KHz crystal of which time base is divided to provide addressable 4-bit I/O data for Seconds, Minutes, Hours, Day of week, Date, Month, and Year. Data access is controlled by 4-bit address, chip selects (CS0, CS1), WRite, ReaD, and ALE. For this system, ALE is stuck to High state.

The Internal Control Register D, E, and F provide for 30 Second Error adjustment, Interrupt Request (IRQ Flag) and Busy status bits, clock Stop, Hold, and Reset Flag bits, 4 selectable Interrupt rate are available at the STD.P (Standard Pulse) output utilizing Control Register inputs T0, T1 and the ITRP/STND. The chip can operate in a 12/24 hour format and Leap Year timing is automatic.

The chip has two chip selector; one (CS0, U10 pin 2) is active Low and is connected to one output of the decoder (U6 pin 9), and the other (CS1, U10 pin 15) is active High which operates with Level detector of memory back-up. The second chip selector prevents the internal data from being damaged while power failure. One failure of two chip selector keeps the chip from being approached.

The address ports select the related internal register and reading/writing may be selected by activating RD or WR signal. A0 to A3 of CPU address bus are connected and they select the internal buffer to be approached. With the buffer selection data bus D0 to D3 can be used data to write and data to read. For the detail register access, refer to the system control map.

The electrical characteristics of this chip are as follows:

Maximum Supply Voltage	from - 0.3V to 7.0V
Operating Voltage	from 4.0V to 6.0V
Standby Supply Voltage	from 2.0V to 6.0V
Input High Voltage	2.2V minimum
Input Low Voltage	0.8V maximum
Output High Voltage	2.4V minimum
Output Low Voltage	0.4V maximum
Input Capacitance	5 pF typ at 1MHz
Current Consumption VCC=5V	30 μ A maximum
VCC=2V	10 μ A maximum

~~The time base of the real time clock is used for various alarms, and the current clock display.~~

~~To initialize the real time clock, you may use the user-program 55 (Time and Date).~~ And, to protect the real time clock running from power failure, you should move the shunt pin SP38 on main board to ON after installation.

To adjust good oscillation, CPD is equipped with two variable capacitors and these capacitors are adjusted in factory. Do not access the variable capacitors unless you have a trouble with the oscillation.

MEMORY BACK-UP CIRCUIT

To protect the memory data and the real time clock data while power failure, the memory back-up circuit is prepared. The circuit consists of Ni-Cd battery, level detector, some gates and diodes, backup ON/OFF switch, and some passive devices.

The shunt pin SP38 on main board is selected to OFF at the factory, for preventing the battery power from consumed while shipment and at the warehouse, which enables the immediate operation after installation. Therefore, you should move the shunt pin to ON position immediately after installation. Otherwise, the consumer data and the real time clock must be volatile at power failure.

The main device is the Ni-Cd battery, which is a rechargeable battery and has a smaller capacity than lithium battery. Some products use the lithium battery and guarantee the longer backup time but it can not be recharged. The battery provides 60 mA_H at maximum and the capacity may decrease compared to time. The Ni-Cd battery for memory backup has three cells and each cell provides 1.2V level. The three cells are connected serially and it supplies 3.6V to backup. The discharge characteristic is some difficult to express but it can be approached with approximation. The system uses 60mA_H capacity battery and 20% of the capacitor may be regardless owing to the reverse loss. Then, the battery capacity to supply is about 48mA_H. With this value, you may guess the duration of backup.

For calculating the duration, the load should be considered. The main load is the power consumed at the static RAM and the real time clock chip. Here, the calculated output may have a large deviation owing to the power consumption of the chips.

The manufacture of SRAM says that the standby power consumption is 2uA typical, 100uA maximum. The difference between the typical value and the maximum is too large. And the supplier of RTC chip guarantees only the maximum consumption is 10uA. Considering with the above data, the maximum load is about 110uA and the typical load is some micro-ampere regardless of the consumption at the gates and passive devices. The difference is based on the lot of semiconductor process.

Considered with the maximum load, the duration is about 436 hours (18 days) and the duration is about 4800 hours (200 days) considered with the typical. The difference is too large and it is difficult to test the practical system. Our factory guarantees three days for the memory backup.

To charge the battery 5 volt power is fed through the diode D19 and the resistor R55. The diode prevents the reverse flow while power failure and the resistor reduces the inrush current and prevents over-charge. The practical power level to charge the battery is about 4.0V and to feed the higher level for charging results from the battery characteristic. Same level power will not deliver any energy to the battery and the charging time becomes too long.

NETWORK

The system is equipped with network for switching all kinds of calls. There are so many kinds of calls and handling methods. But, in the view of hardware, they may be simplified; outside line calls, intercom calls, tone services, and the additional feature services.

The network is composed of cross-point chip M3494. In addition, Tone network is prepared for providing Dial tone to single line telephones. The system uses Space Division Exchange which is usually called as analog system. Space division network becomes the old technology nowadays. Most of popular system is equipped with Time Division Network which enables to provide more powerful features to users but it is more expensive than space division network. Space Division Network is mainly applied owing to the cost. But one or two years later, all the system may use Time Division Network for the powerful service and the flexibility. Some of the current systems which consist of time division network operate awkwardly and it seems a pearl to a pig.

Space Division Network is mainly composed of cross-point chips which control the path by connecting/disconnecting the related cross-point simply. This system uses M3494B2 which is supplied only by SGS. The electrical characteristics are as follows:

M3494 contains a 16 by 8 array of cross-point together with a 7 to 128 line decoder and latch circuits. Anyone of 128 switches can be addressed by selecting the appropriate 7 input bits. The selected switch can be turned on or off by applying a logical one or zero to the data in and the strobe input at logical one. A reset signal can be used to turn off all the switches together when it is set at logical one.

The input pin VG shifts the logic level of the digital inputs. It allows one M3494 supplied between VBB and VDD to have input logic levels equal to VG and VDD. M3494 can handle analog signals with an amplitude equal to the voltage power supply. The system uses 40 lead DIP plastic package.

Supply Voltage, VDD	+ 5.0V $\pm$ 10 %
VBB	- 5.0V $\pm$ 10 %
Operating Temperature	0 to 70 °C
Supply Current, reset	1mA maximum
Crosspoint, On Resistance	60 Ω typ, 100 Ω max
Crosspoint, Δ On Resistance	6 Ω typ, 10 Ω max
Crosspoint, Off Leakage	$\pm$ 3 uA max
Controls, Low Input Voltage	0.8V max
Controls, High Input Voltage	2.4V min
Crosspoint, Frequency Response	50MHz max
Crosspoint, Sinewave Distortion	1 % max at 1KHz
Crosspoint, Feedthrough	- 90dB min at 10KHz
Frequency for Signal Crosstalk	2MHz typ, 1MHz max at 40dB attenuation 5KHz typ at 110dB attenuation

The structure of Space Division Network is a matrix.
Sixteen (16) rows are used as follows.

X0	STN1: 1st Station Speech Path
X1	STN2: 2nd Station Speech Path
X2	STN3: 3rd Station Speech Path
X3	STN4: 4th Station Speech Path
X4	STN5: 5th Station Speech Path
X5	STN6: 6th Station Speech Path
X6	STN7: 7th Station Speech Path
X7	STN8: 8th Station Speech Path
X8	MFR1: 1st DTMF Receiver
X9	MFR2: 2nd DTMF Receiver
X10	MFR3: 3rd DTMF Receiver
X11	MOH : Internal/External Music Source
X12	MFS : DTMF Sender
X13	DOOR : Door Phone Speech Path
X14	PAG : Paging Speech Path
X15	CPD : Call Progress Decoder

16 rows of crosspoint chip are connected each other, which provides the common speech paths. 8 columns of crosspoint chip are allocated to ports, that is, trunks, and common speech path. The ports may be connected through the above rows.

The sum of calls is 3 at maximum. The combination is so many but you can understand it as the maximum number of ports, trunks or stations, of which calls are accomplished simultaneously is 6. The trunks are blocked when all of the common speech paths are used, but the number is sufficient on exchange probability view.

The port connections of base board are as follows:

Y0	C.O1: 1st Trunk Speech Path, Loop-start
Y1	C.O2: 2nd Trunk Speech Path, Loop-start
Y2	C.O3: 3rd Trunk Speech Path, Loop-start
Y3	TONE: Tone Path
Y4	MOH : Music Source Path
Y5	J1 : 1st Common Speech Path
Y6	J2 : 2nd Common Speech Path
Y7	J3 : 3rd Common Speech Path

All the necessary connections are described. Any call can be accomplished with connecting the related ports through any free common speech path.

To control the network is accomplished with the data buffer, 74HCT374 U8 and CPU port. The cross-point address and ON/OFF control data are latched at the data buffer and the related port of CPU selects cross-point chip. The data buffer is also used for selecting the cross-point and controlling the switch at tone network. To control Tone network is described later.

To latch the data to the buffer, I/O address 0F001H is activated with the data. The lowest significant bit D0 is the control bit and the high level connects the related cross-point and the low level dis-connects the cross-point. Each cross-point can be selected with D1 to D7. D1 through D4 selects one of 16 rows and D5 through D7 selects one of 8 columns. After latching the data, you can select chip by enabling port1.0. The detail control map is already described. Refer to System Control Map.

TONE GENERATOR & TONE NETWORK

Tone Generator provides the dual frequency signal for indicating call progressing to users. That is usually called as Audible indications. There are so many kinds of tones provided by a exchange system; Dial Tone, Busy Tone, Ringback Tone, and Reorder Tone, etc. Most of PBX systems are equipped with the different dual frequency signals for the applications. But, most of Key Telephone Systems provide one dual frequency signal for them, of which cadences, ON/OFF period, are adjusted differently for indications. The system is also equipped with one dual frequency generator for all kinds of call progressive tones.

The generator is composed of Wien Bridge Oscillator which is commonly used owing to its reliability and simplicity. Any signal amplifier can be used for Wien Bridge Oscillator and two OP-AMP are used for generating the dual frequency signals and one OP-AMP is used for mixing the signals and adjusting the level.

In Wien Bridge Oscillator, the negative feedback stabilizes the oscillation and the positive feedback determines the frequency oscillated. One OP-AMP generates the low frequency signal of which frequency is determined as follows:

$$\text{Low Frequency} = 1/(2\pi * TL)$$

TL is the root value of $(C61 * C62 * R25 * R24)$

$$= 358 \text{ [Hz]}$$

And the other OP-AMP generates the high frequency of which frequency is determined as follows:

$$\text{High Frequency} = 1/(2\pi * TH)$$

TH is the root value of $(C59 * C60 * R30 * R31)$

$$= 425 \text{ [Hz]}$$

Two Wien Bridge Oscillators generate the dual frequency signals of which frequencies are 358 Hz and 425 Hz, and they are mixed with the small signal amplification circuitry composed mainly of OP-AMP. The input resistors and the feedback resistor determine its gain and the low and high cutoff frequencies can be decided with the capacitances and resistances.

The low cutoff frequency is determined about 1.59Hz and the high cutoff frequency is about 67.73KHz. The frequency characteristic is strangely determined and it decreases the quality but will not effect the system operation but it may result in low or high frequency noise at some systems. You may change the input and feedback capacitors if necessary.

The generated tone signal is fed directly to network for call progressive tone signals, that is, Dial Tone for keysets, Ringback tone, Busy Tone, Reorder Tone, etc. The output impedance of OP-AMP is all-most GND and the tone source can drive some ports at the same time. Tone signal swings at the GND reference because the non-inverting terminal of the mixer is connected to GND.

The generated tone signal is also fed to the six small signal amplifiers which are for the dial-tone supplies to single line telephones and some tie lines. For keysets, Dial Tone source may have low impedance because dialing at keysets is supported with data communication. But, at single line telephones. Dial Tone source should have the terminating impedance, otherwise, the co-operated DTMF receiver can not detect dialing owing to the sink of the DTMF signals from single line telephones and tie lines. For the terminating impedance, the small signal amplifiers are interfaced and Tone Network is required.

The system uses 1.8K ohm resistor for termination and it results in signal amplification, because the level of tone signal decreases without amplification. The gain is determined with the rate of the feedback resistance and the input resistance. And, 2.5 volt reference is fed to the non-inverting terminal for tone network which has the path from GND to 5V.

Three amplifiers are prepared for supplying dial tones with DTMF receivers.

Tone Network is composed of one 22100 cross-point chip which has four by four cross-point matrix. Tone Network is supplied with 5 volt and GND, of which signal path is from GND to 5 volt. Therefore, all the signals through tone network should have the levels from GND to five volts and they are clamped to 2.5 volt reference.

The rows of cross-point matrix are connected to the amplifier outputs via the terminating resistors and the columns of cross-point matrix are connected to network with DTMF receivers.

The dial tone supplier to single line telephones should not have any distortion which may disturb the operation of DTMF receivers.

If you have any trouble to use a single line telephone of which signalling is DTMF, then approach to the dial tone amplifiers. They do not have any feedback capacitor, which may generate the high frequency distortion and it disturbs the operation of DTMF receivers. You may add the feedback capacitor, of which capacitance is 2.2 nF. So far, we are not experienced in the above trouble, but the absence of the feedback capacitor can not be recommended. In addition, the absence of the feedback capacitor may provide high-frequency noise to single line telephones during dial tone service.

The cross-point chip of Tone network has six control terminals; one for chip select and the other five for cross-point selection and ON/OFF control. Chip selection can be accomplished with direct control of the related CPU port; P1.1. And the latched data for Network is multi-used for Tone Network control, 74HCT374 U8; D0 to D3 for cross-point selection and D4 for ON/OFF control. Refer to the system control map for detail. Here, we can be experienced in the designer's deep care for software engineer; inverted control data between Speech Network and Tone Network.

CALL PROGRESS DECODER

Call Progress Decoder monitors the call during auto-redial. The system provides auto-redial feature which enables to repeat the outgoing call automatically if the opposite party is busy. CPD enables the system to detect that the receiving signal is busy tone or not.

The system is equipped with NE5900 for call progress decoder. The chip has sixteen pins for connection and detects Dial Tone, Ringback Tone, Busy Tone or Reorder Tone. The electrical specifications are as follows:

Operating Temperature Range	0°C to 70°C
Power Supply Voltage	4.5V to 5.5V
Input Threshold	- 39dB typ, - 35dB max
Signal Rejection	- 50dB max
Low Frequency Rejection	180Hz max
High Frequency Rejection	800Hz max
High Input Voltage	2.0V to 15V
Low Input Voltage	0V to 0.8V
High Output Voltage, 0.5mA	VDD - 0.4 min
Low Output Voltage, 1.6mA	0.4V max
Tri-state Leakage	3.0uA max
Input Impedance	1 M Ω min
Envelop Response Time	38mS typical

The call progress decoder chip will not operate well because the exchange system which our system may be connected to may not be equipped with the standard tone supply. To cover this possibility, the system program is prepared to serve the auto-redial feature regardless of the fault of CPD device.

The Call Progress Decoder has to be provided with the external crystal for reference frequency supply, which is driven by the internal oscillator. 3.579545MHz crystal should be connected.

The CPD device is controlled with one chip select, one clear, one data valid, and three data bits. The device can be approached only with chip_select enabling. The Clear pin may be used for initializing the chip status after getting the necessary data and the Data Valid bit indicates the chip has got the valid data based on decoding the signal from the input. The three data pins say what kind of tone is detected. For the detail control, refer to the system control map.

DTMF SENDER

The system is equipped with one DTMF sender which dials with DTMF signals to the outside lines. Generally, DTMF sender provides 16 DTMF signals but only 12 DTMF signals are used commercially. The not-used DTMF signals are for military purpose.

KA2413B is prepared for sending DTMF signals. The device is supplied only by Samsung Semiconductor and its electrical features are as follows:

Operating Temperature	- 20 °C to 70 °C
Storage Temperature	- 55 °C to 150 °C
Maximum Power Dissipation	400mW
Operating Voltage	4.3V to 9.0V
Operating Line Current	10.0mA max
Standby Line Current	250uA max
Tone Output Frequency	
1st low frequency	697Hz $\pm$ 1.0%
2nd low frequency	770Hz $\pm$ 1.0%
3rd low frequency	852Hz $\pm$ 1.0%
4th low frequency	941Hz $\pm$ 1.0%
1st high frequency	1209Hz $\pm$ 1.0%
2nd high frequency	1336Hz $\pm$ 1.0%
3rd high frequency	1477Hz $\pm$ 1.0%
4th high frequency	1633Hz $\pm$ 1.0% (Military)

Signal Level : High and Low frequency levels can be respectively adjustable

Pre-emphasis : Can be adjustable

Total Harmonic Distortion - 31.0dBm

Standby Output Noise - 80.0dBm

Harmonics 300 to 3400Hz - 33.0dBm

3.4 to 50KHz - 33.0dBm

above 50KHz - 80.0dBm

Start-up Time 3mS typ, 5mS max

The device uses the external crystal for the source frequency of which value should be 3.579545MHz. The device has ~~some fortes: The pre-emphasis can be adjustable, and it operates with low harmonics and fast start-up time.~~ But, it also has a defect with the internal amplifier. Viewing the structure of the device, two individual frequencies are mixed and amplified but the amplifier generates the high frequency distortion owing to the co-operating of the feeding power and signal output.

~~To overcome the defect, the system does not use the internal amplifier and apply the two external amplifier for the signal amplification.~~

This application enhances the operation of DTMF sender.

The device has nine control terminals; one for mute control and another eight for DTMF signal selection to be generated. The mute control is not used and the signal selection can be approached through a latch. Owing to the continuous operation without mute control, the latched data is all for control of DTMF Sender.

74HCT374 (U20) is 8-bit octal transparent latch which is selected with the first and second decoders whose address is [9000H]. 8-bit data latched at this buffer selects a DTMF signal according that D0 to D3 selects the column frequency and D4 to D7 selects the row frequency. Refer to the system control map for detail control.

The system is equipped with this one DTMF Sender for all trunk interfaces; 3 outside lines at maximum, that is, this DTMF Sender should serve all the outside lines which are selected to DTMF lines by user programming. And the duration of DTMF signal is assigned by user programming.

The generated DTMF signal is amplified with the first and second external amplifiers to adjust the high and low frequency group level. The first amplifier frequency characteristics are as follows; 15.9Hz low cutoff frequency and no high cutoff frequency. The second amplifier frequency characteristics are determined as follows; 258Hz low cutoff frequency and 13.40KHz, which are all selected without care. The low cutoff frequency may be recommended about 300Hz and the high cutoff frequency to 3400Hz.

The mis-selection of frequency pass-band will not result in any critical mis-operation. Because, all the operations of the DTMF generator are fully tested at the factory before shipment.

You may see the resistor R34 which is connected between the second amplifier and the speech network. It is a source impedance of DTMF generator, which is specified at the regulations of tele-communication equipment. The resistance can be determined by measuring the AC impedance during DTMF sending. The trunk interface and network effect on selecting the resistance. AC impedance during DTMF sending should be 600 $\pm$ 10% specified at the most regulations.

DTMF sender is mainly for sending DTMF signals to outside lines which are the data to select the opposite subscriber at the exchange. To send the addressing signals, DTMF or Dial Pulse may be assigned. The system serves both of the addressing signalling for each line assignment by user programming. To send Dial Pulse will be described later at trunk interface circuit descriptions.

DTMF RECEIVERS

The system is equipped with DTMF receivers for detecting DTMF signal from single line telephones.

One day, Dial pulse signalling is only the communication method for addressing at exchange before the advent of electronic technology.

Nowadays, DTMF signalling is mainly method for addressing and all of single line telephones are equipped with DTMF dialer. Therefore, the system provides the feature to detect both of signalling from single line telephones and the specific outside lines. To detect Dial Pulse may be described later.

MT8870C is used for receiving and decoding DTMF signals. The specifications guaranteed by supplier are as follows:

MT8870C is a complete DTMF receiver integrating both the bandsplit filter and digital decoder functions, fabricated in double poly CMOS technology. The filter section uses switched capacitor techniques for high and low group filters and the decoder uses digital counting techniques to detect and decode all 16 DTMF tone pairs into a 4-bit code.

Operating Voltage	4.75V min, 5.0V typ, 5.25V max
Operating Temperature	- 40 °C to 85 °C
Crystal Clock Frequency	3.579545MHz typ
Standby Supply Current	100uA max
Operating Supply Current	3.0mA typ, 9.0mA max
Power Consumption	15mW typ, 50mW max
High Level Input, control	3.5V min
Low Level Input, control	1.5V max
Input Leakage Current	0.1uA typ
Pull-up Current, source	7.5uA typ, 20uA max
Pull-down Current, sink	15uA typ, 45uA max
Input Impedance (IN+, IN-)	10M Ω typ
Steering Threshold Voltage	2.2V min, 2.5V max
Low Level Output, control	VSS + 0.03V max
High Level Output, control	VDD - 0.03V min
Output Low Current, sink	1.0mA min, 2.5mA typ
Output High Current, source	0.4mA min, 0.8mA typ
Vref Output Voltage	2.4V min, 2.7V max
Vref Output Resistance	10K Ω typ
Input Leakage Current, Gain AMP	100nA max
Input Resistance, Gain AMP	10M Ω min
Input Offset Voltage, Gain AMP	25mV max
Power Supply Rejection, Gain AMP	50dB min at 1KHz
Common Mode Rejection, Gain AMP	40dB min
DC Open Loop Gain, Gain AMP	32dB min
Unity Gain Bandwidth, Gain AMP	300KHz min
Output Voltage Swing, Gain AMP	4.0Vpp min
Maximum Capacitive Load, Gain AMP	100pF max
Maximum Resistive Load, Gain AMP	50K Ω max

Valid input level, DTMF	- 29dBm min, 1dBm max
Negative Twist Accept, DTMF	6dB max
Positive Twist Accept, DTMF	6dB max
Frequency Deviation Accept, DTMF	$\pm 1.5\% \pm 2\text{Hz min}$
Frequency Deviation Reject, DTMF	$\pm 3.5\% \text{ min}$
Third Tone Tolerance, DTMF	- 16dB typ
Noise Tolerance, DTMF	- 12dB typ
Dial Tone Tolerance	$\pm 22\text{dB typ}$

*** Valid Tone Duration	40ms
Valid Pause Duration	40ms
Valid Dial Tone	$(350 + 440\text{Hz}) \pm 2\%$
Error Rate	better than 1/10000

Tone Present Detect Time	5ms min, 11ms typ, 14ms max
Tone Absent Detect Time	0.5ms min, 4ms typ, 8.5ms max
Tone Duration Accept	40ms max
Tone Duration Reject	20ms min
Inter-digit Pause Accept	40ms max
Inter-digit Pause Reject	20ms min

Propagation Delay (St to Q)	8us typ, 11us max
Propagation Delay (St to StD)	12us typ, 16us max
Output Data Set-up (Q to StD)	3.4us typ
Propagation Delay (TOE to Q En)	50ns typ
Propagation Delay (TOE to Q Dis)	300ns typ

Crystal frequency	3.5759MHz min, 3.5831MHz max
Clock Input Rise Time	110ns max
Clock Input Fall Time	110ns max
Clock Input Duty Cycle	40% min, 50% typ, 60% max
Capacitive Load	30pF max

Detecting hook-off in single line interfaces, DTMF receiver may be connected to Network with Dial tone. After receiving the first digit, Dial tone is dis-connected and DTMF receiver continues to detect the digits from single line telephones or the specific lines to receive the addressing digits or to prevent the subscribers from dialing a toll. For Dial Pulse lines or telephones the device will not operate.

The system has three DTMF receivers.

It is difficult to receive DTMF signals from all the possible ports at the same time owing to the restricted number of receivers. The maximum port number handled at the same time equals to the number of DTMF receivers.

Therefore, the subscriber which wants to make a call can not dial any digit when all the DTMF receivers are already assigned to others.

Tele-communication probability says that the previous occasion will not happen frequently.

To control DTMF receivers on Base board, three decoded addresses, three status detectors, and four read data pins are used. The power-down and inhibit mode are prevented from operation, of which the related pins are stuck to GND.

CPU monitors periodically DTMF receivers whether they have detected any valid DTMF signals with the read buffer. 74HCT244 (U15) is used to detect the valid signal, of which inputs are connected to three StD pins of receivers. StD pin of receiver may rise to HIGH when the chip received a valid DTMF signals. The inputs are pulled up with the external resistor array.

After detecting StD, CPU can read the DTMF data registered in the chip. Three control signals decoded by the second decoder can select one of DTMF receivers to output DTMF data. The control pin is called as Three State Output Enable which can be activated by High state. Active_high logic requires the additional inverter because the output of decoder is Low_state.

DTMF data can be read through the transparent data buffer. 16 DTMF signals can be detected by the receivers and four of them must not be used commercially.

TRUNK INTERFACES

The system is equipped with one kinds of trunk interfaces which is connected to the other systems or the central office. Key Telephone System is a small private exchange equipment, of which connections are mainly for its subscribers and the outside lines. Trunk interface are the interface circuitry for the connection to the outside lines and some kinds of trunk interfaces are commonly used.

Loop-start trunk interface consists of Surge Protection circuitry, Loop Relay, DC by-pass, Loop/Ring Detector, and Speech Transfer circuitry.

Loop-start trunk has two outside line connections which are called as Ring and Tip terminal. Ring terminal receives the ring signal and it is a reference line for signalling and speech. And, Tip terminal receives the hot signals. Generally, the terminals of Loop-start trunk has no polarity and the previous description on their roles can be indifferent.

Anyway, loop control is the main signalling at loop-start trunk. In idle state, the loop is dis-connected and the loop becomes accomplished for starting of signalling. After the loop maid, Dial Pulses or DTMF signals are transmitted for addressing. The exchange equipment accomodating the line may detect the address signals and it operates to connect the originate to the opposite according to the addressing signals. It describes the outgoing procedure of the loop start trunk. And, its incoming procedure is as follows; the exchange generates ring signals and it can be detected at this interface and the system gives the ring signal to the assigned stations.

Surge Protection circuitry is composed of two arrestors, two fusable resistors, and one varitor and it protects the system from any surge or high voltage. Two arrestors are connected between Tip and Earth and Ring and Earth, which blocks any longitudinal high voltage. The capacity of the arrestor is 300 volts and any signal of which longitudinal voltage is below 300 can be transferred but any signal above 300 volts may be clipped and the arrestor will be short at that case. As above, two arrestors protect the system from any longitudinal high voltage.

One varistor has 390 volt capacity and it is connected between Tip and Ring. It protects from any metallic surge. The signal above 390 volt may be clipped and two fusable resistors will work if the energy is too high. The fusable resistors work as fuses at that case. The fusable resistor has 10 ohm and .25 watt capacity. The difference between fuse and the fusable resistor is that the fusable resistor can be restored and the fuse will blow. The fusing time of the fusable resistor varies based on the feeding energy, that is, 10 watt input may activate the fusing operation within 3 seconds and 5 watt input may activate within 14 seconds. And the maximum flame voltage is 350 Vrms or DC. Regarding with the flame voltage and the varistor, any metallic input below 1090 volts may clipped and dis-connected for protection and the input above 1090 volts may blow the fusable resistors. A large energy input may blow the fusable resistors and arrestors but it will not happen frequently.

As above, the surge protection circuitry protects the system from any large signal input via the trunk lines owing to a surge or the other cause. In a frequent lightening site, it is recommended that the additional surge suppressor should be connected parallel to the lines. And, grounding the system is essential to the operation of the circuitry.

After the surge protection circuitry, the lines are connected to loop relays and the relays for power failure transfers. Power Failure Transfer operates to connect the loop-start lines to the related SLT lines through the relay when power failure. The system provides three power failure transfer lines for emergency and the operation will be described later.

~~One relay driven with plus 24 volts is prepared to connect or dis-connect the loop.~~ The one form relay controls the loop and it also generates dial pulses if assigned. The relay is driven by the relay driver, UCN5801A. As described, two signalling method are used at loop-start trunk, Dial Pulse and DTMF. DTMF signals are transmitted with the DTMF sender through network, of which operation is already described. But, Dial Pulses are generated with the loop relay control. 40 milli-second make and 60 milli-second break are used generally for one pulse and the time ratio is manipulated by program. The relation between digit and pulse number is as follows:

Digit 1	one pulse
Digit 2	two pulses
Digit 3	three pulses
Digit 4	four pulses
Digit 5	five pulses
Digit 6	six pulses
Digit 7	seven pulses
Digit 8	eight pulses
Digit 9	nine pulses
Digit 0	ten pulses

The pulse make/break ratio can be adjusted by user programming. To generate dial pulses or DTMF signals is determined by user programming and it is up to the exchange equipment. DTMF signalling is the advanced method and it provides the higher service than dial pulse signalling, but the old exchange equipment can not receive any DTMF signal. At that case, you should assign the lines to Dial Pulses.

Parellel to the loop relay, ~~ring signal path~~ is provided with a resistor, a capacitor, and two zener diodes. These components decides the ring impedance and the path transfers the ring signal to the following circuit where it may be detected. Two 30 volt zener diodes cut off the ring signals to the adequate level to detect and the resistor and the capacitor provide the ring impedance. Especially, the capacitor gives the ring capacitance which may be used for detecting the installation of the equipment through the lines by central office or PABX.

Hybrid device is connected after the loop relay, which bypasses DC and transfers AC signals. The resistance is about 200 ohms to 400 ohms which is specified at the telecommunication regulations. Terminating the loop is made with this DC bypass hybrid. The hybrid part number is KP0039SA and it is designed by Samsung Electronics. The internal architecture is simple and the detail operation will not help you because you can not have access to the device. The hybrid has a insertion loss but it may be indifferent owing to the minute loss in voice band.

Attached to DC bypass hybrid, the photo-coupler, PC817, is prepared to detect the loop or ring signals. The secondary part is connected to the read buffer, 74HCT244(U15), of which data is read periodically and analyzed by CPU. The diode may generate the photo signal to the secondary gate if there is a ring signal on hook or DC is fed to the ring and tip terminal off hook. The photo-coupler is used for power isolation between the trunk interface and the system, instead of direct detecting.

The transformer, ST-1C is a audio transformer which isolates the system from the trunk interface and its turn ratio is designed to 1:2, which reduces the loss on the network. The audio signal may be transferred from or to network through the clipping circuit which is composed of two zener diodes of which zener voltage is respectively 4.3V. The zener diodes, 1N749A protect the network from any over-voltage, of which signal range is recommended from minus 5 volts to plus 5 volts.

This system has 3 loop-start trunk interfaces. 3 loop relays are driven by the driver, UCN5801A U17. The driver has the internal latch and the darlington array to drive, and the darlington array has the open drain feature. 3 photo-coupler outputs are connected to the read buffer, 74HCT244 U15. The additional resistor and capacitor are required because the output of the photo-coupler is open-collector.

KEYSET INTERFACES

Keyset is the proprietary equipment of the system and it may not operate with the other system. Samsung Electronics provides AS-11 series keysets for the system. In addition to this, AS-30 series and SKP-816H keysets can be accommodated.

Single line telephones can be accommodated but keysets provide more powerful and useful features to users.

Keyset interface is for connecting the keyset to the system. The interface is composed of data path and speech path; the data path enables the data communications between the system and the keyset, and the speech path is for the speech signal transmission. Therefore, four wires are required to install one keyset for two wires become one path. This is the architecture of the analog system.

In the digital system, only one path is enough to install the digi-phone because the data and the speech signals are transmitted via one path modulated and shared on time basis.

The data communications results in the more powerful and useful features: DSS, DTS, BIF display, and on-hook services, etc.

Hook switch and all button data are transmitted from keyset to the system and the system analyzes the data and the status and sends the control data to keyset; LED data, LCD data, and speech control data, etc.

With regard to a keyset, the data communications are asynchronous and serial. Each bit duration is 3ms. The sending data to keyset are as follows:

[Sending Data Format to Keyset]

1	Start bit	High state
3	Network ID	MSB first, keyset network control data
8	First Data byte	MSB first
8	Second Data byte	MSB first
2	Waiting bits	Low state

The data to keyset are inverted at the de-modulation circuit in keyset and the sending data are composed of 22 bits including waiting bits as above. After sending the data the system receives the data from keyset.

[Receiving Data Format from Keyset]

1	Start bit	Low state
1	Parity bit	Even Parity Check
7	Data bits	MSB first
2	Waiting bits	High state

The system receives 11 bits from keyset and the parity bit is for checking any fault in data communications.

As above, one data monitor is accomplished and immediately after receiving the data from keyset the system is sending its data again. The procedure is repeated continuously regardless of keyset hang-on or hook-off.

Sending/receiving data are totally composed of 33 bits and it requires 99ms.

With regard to a keyset, the data communications are accomplished with serial and asynchronous format. But, ~~the data to all of keysets are transmitted/ received at the same time.~~ For example, all of starting bits are transmitted to all of keysets at the same time. Therefore, the data monitor period to a keyset and the total period are all the same, 99ms.

The format of data communications is some different with the standard serial interface, which is designed for the primitive system and becomes the standard protocol of the small and middle size system made by Samsung Electronics.

The data-com circuitry consists of TX buffers, RX buffers, modulation/ demodulation circuits, and power isolators.

74HCT374, a latch buffer is applied to the TX buffer. All the simultaneous bits to keysets are latched and transmitted through this buffer. The Most Significant Bit is for the leading keyset and one TX buffer is required for 8 keysets at maximum.

74HCT244, a read buffer is used for the RX buffer. All the simultaneous bits from keysets are latched and read through this buffer. The Least Significant Bit is allocated to the leading keyset and one RX buffer is required for 8 keysets at maximum.

The loop length for the keyset can be extended to 400 meters at maximum and the data can not be detected without modulation. Therefore, the data is modulated and transmitted and demodulated and detected.

The modulation/demodulation circuits come to the hybrid device, HYB-1.

The modulation/demodulation circuits for four keysets are mounted to one HYB-1. The internal circuit is simple.

The modulation is accomplished with differentiating the pulse data. The transition from low to high is converted to high peak and the transition from high to low is converted to low peak of which time constant is determined by the resistor and the capacitor. The minimum width between one peak and the other is 3ms owing to the data rate and the time constant is determined to 1ms.

The modulated signal is transmitted through the transformer, 5692 which is applied for the power isolation.

The data from keyset is also the differentiated form and received through the same transformer. The modulated signal is converted to the pulse with the demodulation circuit. The signal level is detected and the high/low thresholds determine the output to High/Low data. The noise margin is ± 0.8 volt which is determined by the high/low threshold levels.

Two OP-AMP's are applied to modulate/demodulate the data and the supply voltage is 12 volts which increase the signal level and enhance the data transmissions. HYB-1 hybrid device has four modulation/demodulation pairs and two HYB-1 hybrid devices are required for 8 keysets.

The internal circuit diagram of HYB-1 hybrid device must not be necessary for you can not approach the internal parts of the device.

The data-com circuitry is very simple and efficient owing to the low cost. The system uses the differentiated peak signal to transmit as described, and it may be the source of ticking noise at the speech path at the long loop. At that case, the twisted pair cable will reduce the noise.

The speech path is simply composed of the isolation transformer (ST-1C) and the network protection devices. Two zener diodes block and cut down any over-voltage over ± 4.3 volt to protect the network devices. The transformer has 1:2 turn ratio and it is the same device with the transformer applied to the trunk interface, which matches the audio impedance.

The keyset power is supplied by the system via the data and speech path. The system ground is fed through the center-tapped terminal of the speech transformer and the high power about 30 volts is fed through the center-tapped terminal of the data transformer. On the high power feeding line, a thermistor is prepared for short-protection.

This power feeding using the center-tapped terminals has some merits:

- Small size transformer may be available owing to the thin wire.
- Low loss on the line
- Small effect of the power noise

8 keyset interfaces are prepared and 7 of them are the mixed circuits of keyset and single line telephone interfaces. Single line telephone interfaces which will be described later use one path for one telephone and the keyset speech path is mixed with single line telephone interface, which may be determined by moving the related shunt pins.

Refer to the installation and programming manual.

SLT INTERFACE

The system is equipped with the interface circuitry for single line telephones which is the primitive and basic equipment of tele-communications. Most of the current single line telephones operate with loop-start protocol and they may be equipped with the dialers to generate dial pulses or DTMF signals. Before the advent of electronics, mechanic exchange systems serve the tele-communication networks and pulse dialing is the addressing protocol. But, nowadays DTMF signals are popular for the addressing signals which are supported by the electronic systems.

Some telephones are equipped only with pulse dialer. Therefore, the interface is designed to serve two kinds of addressing signals, Dial Pulses or DTMF's.

Single Line Telephone requires two wires; Tip and Ring and all of the necessary transmissions of signalling and speech signals are accomplished through the lines. Two wires are the basic element to transmit any signal which can be easily understood if you have some knowledge. And two wires are one pair which is usually called as one line. Therefore, the popular telephone is called as single line telephone [SLT].

The procedure to originate a call from SLT is as follows:

Hook-off	System detects with loop-termination [Loop-start] System provides Dial Tone System prepares DTMF receiver and SLT pulse detector
Dialing Pulses or DTMF's	System reads the digit through the DTMF receiver or pulse detector System serves based on the receiving digits

Dialing pulses or DTMF signals is determined in the single line telephone and the system can receive any addressing signals. Based on the digits from single line telephones the system serves a intercom call, a outside call, or the other features. The digit assignments and the methods are described at user's guide in detail. Refer to the user's guide if necessary.

The procedure to receive a call is as follows:

Ring signal feeding	System decides to provide the ring signal to SLT for a intercom call or incoming call
Hook-off	System detects hook-off System disconnects the ring signal System connects the speech path

SLT interface is composed of power feeding part, ring signal feeding part, loop/pulse detection circuit, PFT relay, speech transmission circuit, and over-voltage protection devices, and the DTMF receiver can be connected through network components.

The main device of SLT interface is the hybrid component, SLC-01 which is developed by Samsung Electronics. ~~The hybrid component includes power feeding part with speech signal transmission and loop/pulse detection circuit.~~ The regulated DC from the connection board is fed through the hybrid device and its value is about 30 volts varying according to the power input voltage and load. And, the loop/pulse detection circuit in the hybrid device will perceive the loop condition. For detecting the loop during ringing, ring trip circuit is simply attached. The internal detail description on the hybrid component may not help you because you can not approach the internal parts.

Ring signal generated on the connection board may be fed through the ring relay, RY24W-K where the ring control and cadency can be adjusted by CPU. The relay driving voltage is 24 volts and UCN5801A is applied to drive the relay. The ring signal path includes the serial resistors for short protection.

Three SLT interfaces have the power failure transfer relays which are driven by the 24 volt power. 24 volt power-up selects the relay path for normal connection and the power-down activates the path connected to the related trunk line directly.

~~Transformer ST-1C is prepared for power isolation of the speech path which is the same with the transformer in trunk interface for impedance matching and reduction of the network loss. Two zener diodes are attached to protect the network chips from any over-voltage.~~ The primary turn is connected to the network and the secondary turn is connected to the hybrid component.

The result to detect loop/pulse is respectively connected to the read buffer, 74HCT244 and the data are got by CPU.

This system has 8 station interfaces and 7 of them are allocated to the hybrid port. To select keyset or SLT interface is determined by moving the related shunt pins of which informations are described in the installation/programming manual.

Reference] 4 shunt pins are allocated to one hybrid port. You can select easily keyset or SLT for "K" or "N" mark indicates keyset or single line telephones.

One shunt pin is allocated to connecting GND to the center-tapped terminal or not. Connecting GND is for keyset power feeding and opening is for SLT because the power to SLT is supplied through the hybrid device. The other one is allocated to short the both ends of the capacitor which is used for preventing the transformer from saturation when the port is used as SLT interface. But, the capacitor will be a obstacle when it is assigned to keyset interface and it should be short.

The another two shunt pins are allocated to feed the power to SLT and they should be open when the port is assigned to keyset.

MUSIC SOURCES

The system is equipped with two kinds of sources, internal and external. These two sources are selected by shunt pin and connected to network.

The music sources have two names, MOH and BGM according to its usage. Music On Hold (MOH) is the music provided on hold and BackGround Music (BGM) is the music heard at the keyset. But it is provided from the same source, the internal music or the external music source.

The internal music source is basically equipped in the system and is composed of the melody generator, and OP-AMP.

The melody generator, RTS993-8 is applied and its features are as follows:

RTS993-8, MELODY GENERATOR

RTS993-8 is a CMOS LSI designed to play the melody according to the previously programmed information and capable of generating songs with the piano effect. Internal oscillator, tone generator, envelope generator, rhythm generator, ROM, and control logic are the internal composition. The package is the dual-in-line and has 16 pins. The absolute maximum ratings are as follows:

DC Supply Voltage	0V to 5.0V
Operating Temperature	0°C to 60°C
Storage Temperature	0°C to 125°C

And, the operating current is 2mA typically.

It has six songs and the songs are designed to play continuously.

La Reine Deo Saba
For Elise
Santa Lucia
Maiden Pray
Music Box Dancer
Moonlight on the Colorado

A variable resistor(VR1) is connected to the output of Melody IC. The variable resistor is for adjusting the MOH level and its value is set in the factory. For BGM, you should adjust the level at the keyset.

Following the variable resistor, a voltage follower is prepared for the low impedance source, which enables to apply the source to some of trunks or stations at the same time. Otherwise, the cross-talk happens on hold or some independent music sources may be required.

You can install the external music source for MOH or BGM, tape recorder or radio. The system is equipped with the interface for the external music which consists of the isolation transformer. Audio jack is prepared.

The Transformer, ST-1C isolates the power between the external music source and the system and its turn ratio is 1:2 for impedance matching. Two zener diodes protect the network from over-voltage which may damage the network chips. The transferred signals via transformer are fed to OP-AMP input which output is connected network.

Some of tape recorders feed DC voltage to the audio line and you should add a some miro-farad capacitor to block the DC voltage on line. Otherwise, the isolation transformer may be saturated.

DOOR-PHONE INTERFACES

The system is equipped with two door-phone interfaces with lock release controls on the base board. You can not install any commercial door-phone to the system and only the door-phone provided by Samsung Electronic may be available.

Door-phone can be installed near the door or room for monitoring and its operation will be described later.

Four wires are required to connect one door-phone and the additional two wires may be required to control the door-lock if necessary. All the connections are accomplished through MDF.

Two of them are for the speech path and the other two are for the power to activate the door-phone. The speech path is composed simply, one isolation transformer ST-1C and two network-protection zener diodes. And the power for door-phone is fed via a thermistor and 12 volt is used.

The center-tapped terminal of the isolation transformer is used to detect the status of the call button at door-phone.

The user can make a call to door-phone and receive a call from door-phone, too.

The lock release control is composed of a relay and a spark killer. This controls two signal wires connected or dis-connected. Enabling the control means that the relay contact is connected during the programmed period.

EXTERNAL PAGE INTERFACE

The system is equipped with the external page interface which enables the subscriber to make a page through the external speaker. The interface is simply composed as a power-isolated speech path and you should connect the external speaker with the amplifier. Otherwise, the level is too small to hear because the interface is not equipped with any speaker driver.

The connection can be accomplished through MDF with two wires. One transformer ST-1C for power isolation and two zener diodes for network protection from over-voltage are all to be required.

The interface does not have any level adjust device so you may adjust the level at the external amplifier.

POWER REGULATOR

As described, other necessary powers are regulated and supplied from the power board. But the main board has regulator for 24 volt.

The regulator for 24V is a linear regulator, 7824. Its specifications are as follows:

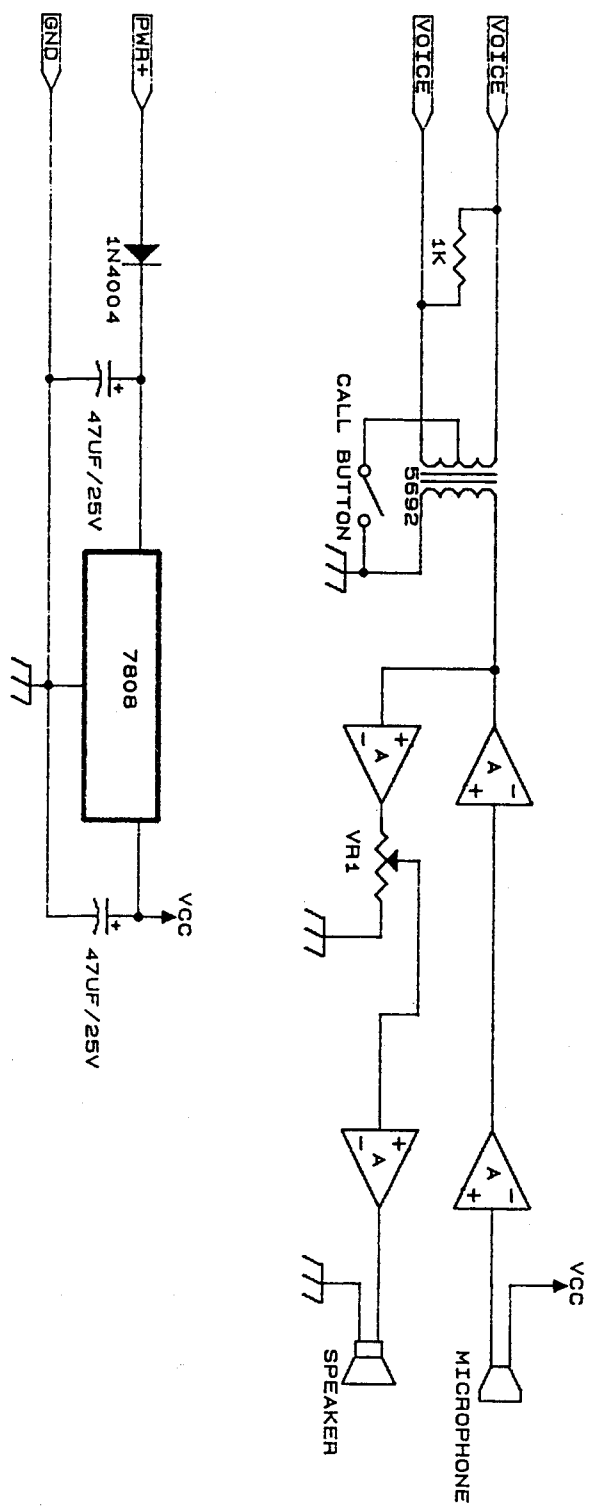
7824. LINEAR REGULATOR

7824 is a monolithic integrated circuits designed as 12 volt output. The regulator employs the internal current limiting, the thermal shutdown, and the safe area compensation.

Input Voltage	40V max
Operating Junction Temperature Range	0 to 150 °C
Output Voltage	22.8V min, 24V typ, 25.2V max
Output Current	5mA min, 1.0A max
Line Regulation	31mV typ, 480mV max
Load Regulation	60mV typ, 480mV max
Quiescent Current	4.6mA typ, 8.0mA max
Ripple Rejection	54dB typ
Dropout voltage	2.0V typ
Output Noise Voltage	10uV/Vo typ
Output Resistance	20mΩ typ at 1KHz
Short Circuit Current Limit	0.2A typ
Peak Current Output	2.2A typ
Average Temperature Coefficient of Output	- 1.5mV/°C typ

24V is mainly used for relay driving.

E. DOOR-PHONE BLOCK DIAGRAM



F. DOOR-PHONE CIRCUIT DESCRIPTION

This section includes the descriptions on the door-phone circuitry. Door-phone requires four wires to connect. Two of them are used for the speech path which has no polarity. The other two wires are allocated to power supply, system ground and plus twelve (12) volts.

Door-phone is composed of the speech circuitry, power supply, and call-button detector.

The speech circuitry consists of speech TX path and speech RX path.

A condenser microphone is used as a transducer from the physical signals, real voice to the electrical signals. The transduced signals are amplified with the first and second amplifier circuits. The power supplied to the amplification circuit is 8 volt DC which is regulated through the regulator.

The output is transferred to the system through the power-isolating transformer, 5692. The termination resistor is 900 ohms.

The speech signals from the system are transferred through the power-isolating transformer, 5692 and terminated with the resistor. The terminated signals are adjusted at the first RX amplifier. At this amplifier, the transmitted signals are prevented from the feedback to the speaker, which is usually called as speech hybrid circuit.

The output of the first RX amplifier is fed to the variable resistor to adjust the level. The variable resistor can not be approached by user but the repair or maintenance engineer may adjust the level by the access to the internal circuits of door-phone. The RX speech signals are fed to the speaker driver, LM386. The speaker will be driven with the output of the driver.

The power supplied from the system is 12 volts, which is regulated to eight (8) volt DC through the linear regulator, 7808. This power is supplied to all of the circuits to operate.

The power should be dis-connected in the system while door-phone is not operated. Otherwise, a howling may happen.

Call button on door-phone can be detected in the system and pressing the button results in grounding the speech path which is detected. One end of the button is connected to the center-tapped terminal of the transformer and the other is connected to door-phone ground connected to the system ground. Therefore, pressing the button connects both ends of the button contacts, which pulls the speech path down to ground.

9. KEYSET BLOCK DIAGRAM

KEY, R.D. ASS'Y, PART

KEYS & ITS
SCANNING CCT

LED'S & ITS
DRIVING CCT

LCD MODULE &
INTERFACE CCT

HANDSET HOOK
S/W DETECT

CONTROL
SIGNAL

CPU & ITS
PERIPHERALS

DATA TX
DATA RX

DATA-COM
CIRCUIT

11.059MHz

47P
47P

HYBRID TX

HYBRID RX

T1
SPEECH TO KSU
POWER -
SPEECH TO KSU

T2
DATA + TO KSU
POWER +
DATA - TO KSU

KEY-TONE
INTERFACE

RING-TONE
INTERFACE

NETWORK
4x4 CROSS-POINT

H/S RX VOLUME
CONTROL CCT

VMS SIGNAL
VMS RECORD

HANDSET TX

HANDSET RX

SPEAKER VOLUME
CONTROL CCT

SPEAKER-PHONE
CIRCUIT

VMS CIRCUIT

0.3W 8OHM
SPK DRIVER

POWER +
5V SWITCHING
REGULATOR

12V LINEAR
REGULATOR

+5V

EXT SPK DRIVER

T3
EXT SPK PATH

C-MIKE

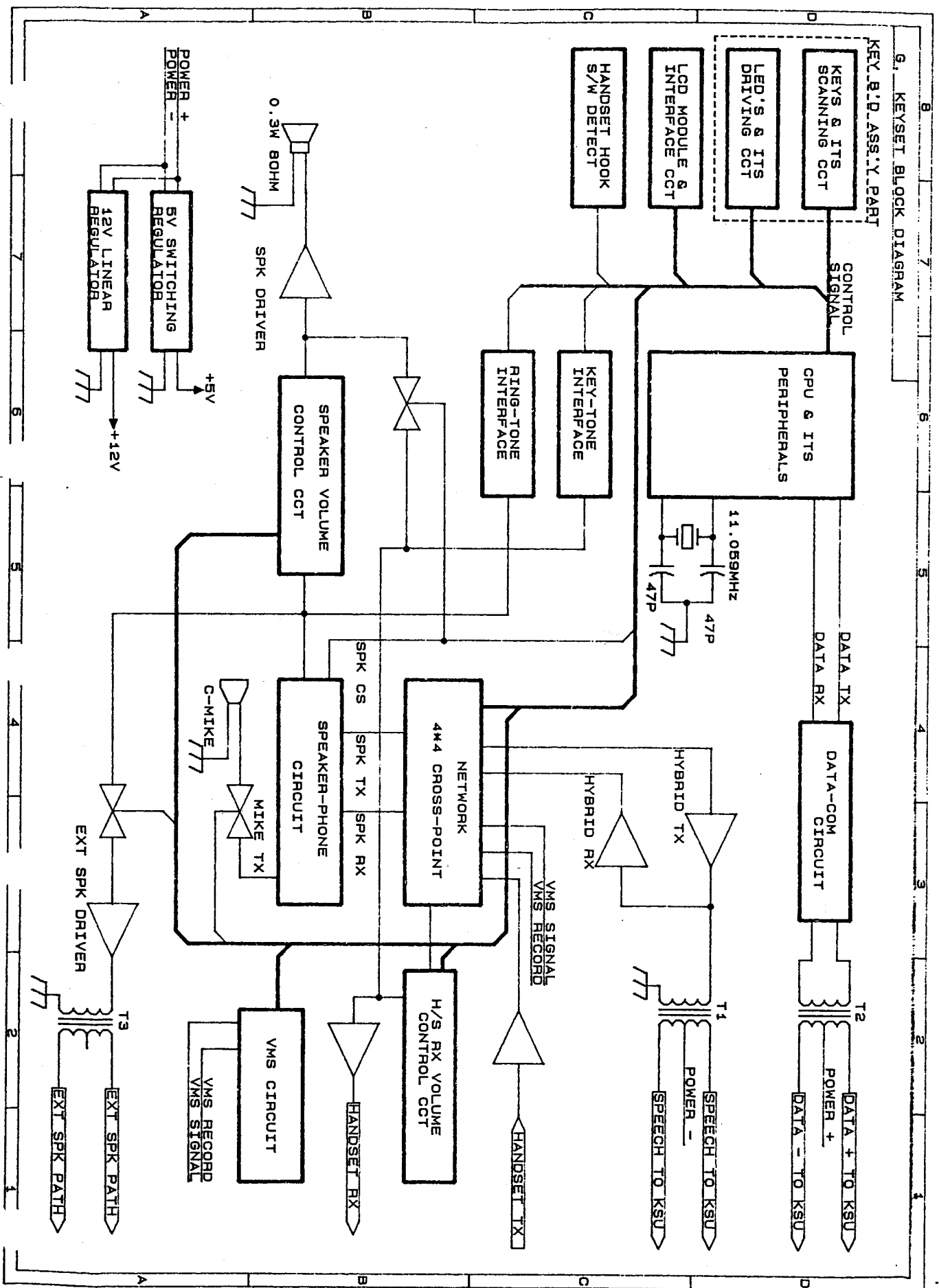
MIKE TX

SPK CS

SPK TX

SPK RX

VMS RECORD
VMS SIGNAL



H. KEYSET CONTROL MAP

Keyset has no any decoder and the addressing concepts are not applied to keyset control.

~~All of the control can be accomplished with port control~~, that is, the control of the related port and data bus, port 0 is enough to handle any specific circuitry in the keyset.

The port controls are as follows:

PORT	DIRECTION	DESCRIPTIONS
Port 0	Input/Output	From P0.0 to P0.7 Used as <u>data bus</u> and pulled externally up by a resistor array, 47K 8R9P.
P1.0	Output	<u>DATA_TX</u> Used for data communication with the system. This port is the data transmit port from keyset to KSU.
P1.1	Input	<u>DATA_RX</u> Used for data communication with the system. This port is a data receiving port from KSU to keyset.
P1.2	Output	<u>VMS_ACCESS</u> Used to latch the VMS interface buffer (74HCT373) with the control data (P0). It is a High Level Latch Enable. The latched data controls VMS processor as follows: D0 <u>VMS_RESET</u> Resets VMS processor with High status. Otherwise, VMS processor runs. D1 <u>VMS_REC</u> Controls Recording/Reproducing. High state indicates Recording to VMS processor and Low state indicates Reproducing from VMS processor. D2 <u>VMS_START</u> Controls to start VMS processor with Recording or Reproducing which is determined by [VMS_REC] state. Before VMS STARTs, the related phrase should be selected and should not be changed until VMS STOP.

PORT	DIRECTION	DESCRIPTIONS
continue		D3 <u>VMS_STOP</u> Controls to stop VMS processor operation, Recording or Reproducing which is determined by [VMS REC] state. If VMS START and VMS STOP signal are activated at the same time, VMS processor will stop. D4 <u>VMS_PHRASE0</u> Refer to the following. D5 <u>VMS_PHRASE1</u> Refer to the following. D6 <u>VMS_PHRASE2</u> Selects VMS phrase from phrase 0 to phrase 7 with the states of VMS_PHRASE0 and VMS_PHRASE1. The product uses five phrases, from phrase 0 to phrase 4. Phrase 0 to phrase 2 are assigned to three voice alarms, phrase 3 is used for the intercom message, and phrase 4 is assigned to outside line message. D7 <u>VMS_EXIST</u> Used to detect the assembly of VMS circuitry. CPU may check it is equipped with VMS circuit or not, and serves differently.
P1.3	Input	<u>VMS_EXIST</u> Used to detect the equipment with VMS processor or not. The port is connected to the output Q7 of the VMS buffer. VMS feature is a set option.
P1.4	Input	<u>VMS_BUSY-FLAG</u> Used to detect VMS processor is operating or not. If VMS processor operates, the port is read LOW. Otherwise, the VMS processor is free.
P1.5	Output	<u>PAGING_EN</u> Used to enable the individual external paging. This port is connected to the analog switch control port which connects or dis-connects the individual external paging path, and LOW state dis-connect the path.

P O R T	D I R E C T I O N	D E S C R I P T I O N S
P1.6	Output	<u>KEY_TONE</u> CPU fluctuates this port to generate 1000Hz pulse train, which is the source signal of Key Confirmation Tone. This port generates or stops key tone signals. Normal High state to sustain high impedance.
P1.7	Output	<u>RING</u> CPU fluctuates this port to generate the various pulse train, which is the source signal of ring tone. This port generates or stops the ring tone signals and the generated signals are characterized to four kinds which are selected with user programming. Normal High state to sustain high impedance.
P2.0	Input	<u>HOOK_S/W</u> Used to detect Hook On/Off. If the user hook the handset Off, the port is read Low. Otherwise, it is read High.
P2.1	Output	<u>WD_CLR</u> Used to clear the Watch-Dog circuit to prevent CPU reset while normal operation with continuous pulse train. In abnormal operation, the port will be sustained High or Low and the circuit generates the reset signal to CPU about 150mS.
P2.2	Output	<u>LCD_EN</u> Used to latch a data to LCD controller mounted on LCD module. The latched data are provided on the data bus [port 0]. High-active.
P2.3	Output	<u>LEDCOL_EN</u> Used to latch a data on the data bus to LED column driver (UCN5801A). High state enables to latch. The latched data are inverted, that is, Low latched datum outs High and enables the related LED's Off, and, High latched datum outs Low and enables the related LED's On, co-operated with the row driving data.

PORT	DIRECTION	DESCRIPTIONS
P2.4	Output	<u>LEDROW.LE</u> Used to latch the data on the data bus to LED row driver (74HCT373). High state enables to latch. Data latched High let the related LED's On and data latched Low let the related LED's Off. This port may approach the D flip-flop's in the driver and their outputs are controlled by [LEDOE] signal.
P2.5	Output	<u>LCDRS/LEDOE</u> This port is multi-used to determine LCD Command/Data and to enable the LED row driver outputs. High state indicates LCD Display Data when [LCD EN] signal is activated and lets the LED row driver disable with high impedance outputs. Low state indicates LCD Command when [LCD EN] signal is activated and lets the LED row driver enabled with its latched data. During activated as LCDRS signal, the port should be manipulated with the data bus before [LCD EN] signal is activated.
P2.6	Output	<u>KSCAN.LE</u> Used to latch the key scanning data to the key-scan driver (74HCT373). High state enables to latch.
P2.7	Output	<u>KSCANOE/LCDRW</u> The port is multi-used to enable Key Scan Latch output and determine LCD Read/Write cycle. High state lets the key-scan latch output disable with high impedance and LCD controller to be read when [LCD EN] signal is activated. Low state lets the key-scan latch output enable and LCD controller to be written when [LCD EN] signal is activated. During activated as LCDRW signal, the port should be manipulated with data bus before [LCD EN] signal is activated.
P3.0	Output	<u>H/S_GAIN1</u> A handset RX gain control port. It operates with [H/S_GAIN2] port for 4-step gain adjustment.

PORT	DIRECTION	DESCRIPTIONS																																				
P3.1	Output	<u>H/S_GAIN2</u> A handset RX gain control port. It operates with [H/S GAIN1] port for 4-step gain variations. <table><tr><td>H/S GAIN2</td><td>H/S GAIN1</td><td>HANDSET RX VOLUME</td></tr><tr><td>L</td><td>L</td><td>Minimum</td></tr><tr><td>L</td><td>H</td><td>2nd Level</td></tr><tr><td>H</td><td>L</td><td>3rd Level</td></tr><tr><td>H</td><td>H</td><td>Maximum</td></tr></table>	H/S GAIN2	H/S GAIN1	HANDSET RX VOLUME	L	L	Minimum	L	H	2nd Level	H	L	3rd Level	H	H	Maximum																					
H/S GAIN2	H/S GAIN1	HANDSET RX VOLUME																																				
L	L	Minimum																																				
L	H	2nd Level																																				
H	L	3rd Level																																				
H	H	Maximum																																				
P3.2	Output	<u>SPK_GAIN1</u> A speaker gain control port which operates with [SPK GAIN2] and [SPK GAIN3] for 8-step gain variations. Speaker-phone RX and Ring Volume can be independently adjusted.																																				
P3.3	Output	<u>SPK_GAIN2</u> A speaker gain control port which operates with [SPK GAIN1] and [SPK GAIN3] for 8-step gain variations. Speaker-phone RX and Ring Volume can be independently adjusted.																																				
P3.4	Output	<u>SPK_GAIN3</u> A speaker gain control port which operates with [SPK GAIN1] and [SPK GAIN2] for 8-step gain variations. Speaker-phone RX and Ring Volume can be independently adjusted. <table><tr><td>SPK G3</td><td>G2</td><td>G1</td><td>SPEAKER VOLUME</td></tr><tr><td>L</td><td>L</td><td>L</td><td>Minimum</td></tr><tr><td>L</td><td>L</td><td>H</td><td>2nd Level</td></tr><tr><td>L</td><td>H</td><td>L</td><td>3rd Level</td></tr><tr><td>L</td><td>H</td><td>H</td><td>4th Level</td></tr><tr><td>H</td><td>L</td><td>L</td><td>5th Level</td></tr><tr><td>H</td><td>L</td><td>H</td><td>6th Level</td></tr><tr><td>H</td><td>H</td><td>L</td><td>7th Level</td></tr><tr><td>H</td><td>H</td><td>H</td><td>Maximum</td></tr></table>	SPK G3	G2	G1	SPEAKER VOLUME	L	L	L	Minimum	L	L	H	2nd Level	L	H	L	3rd Level	L	H	H	4th Level	H	L	L	5th Level	H	L	H	6th Level	H	H	L	7th Level	H	H	H	Maximum
SPK G3	G2	G1	SPEAKER VOLUME																																			
L	L	L	Minimum																																			
L	L	H	2nd Level																																			
L	H	L	3rd Level																																			
L	H	H	4th Level																																			
H	L	L	5th Level																																			
H	L	H	6th Level																																			
H	H	L	7th Level																																			
H	H	H	Maximum																																			
P3.5	Output	<u>SPK_MUTE</u> Used to control the path of micro-phone. The port is connected to the control terminal of the analog switch in series of micro-phone output path.																																				

PORT	DIRECTION	DESCRIPTIONS
continue		High state connects the micro-phone path and enables speaker-phone transmission, and Low state dis-connects the micro-phone path and disables speaker-phone TX. This is called as Speaker-phone Mute control.
P3.6	Output	<u>SPK_CS</u> Used to control the speaker-phone chip [MC34018]. High state blocks to supply the power to the chip and Low state enables to supply the power to the chip to operate.
P3.7	Output	<u>NETWORK_EN</u> Used to latch the network control data to the cross-point chip, CD22100. High-active. The related data should be arranged before the port is activated.

I. KEYSET CIRCUIT DESCRIPTION

This section includes the detail descriptions on the keyset circuits and operations. Proceed with the related circuit diagrams and block diagrams.

Keyset, AS-11 series is composed of so many circuits, that is, CPU and its peripherals, data communication circuit, key scanning circuit, LED driving circuit, LCD and its interface with viewing angle control, handset hook on/off detector, ring-tone generator with digital volume control, key confirmation tone generator, speech hybrid circuit, network, handset interface circuit with digital volume control, speaker-phone circuit, speaker driving circuit with digital volume control, voice message service circuit, external speaker interface circuit, and power regulators.

KEYSET OVERVIEW

AS-11 series keyset is a analog subset which operates behind SKP-308H system made by SAMSUNG Electronics Co. LTD. AS-11 series include four kinds of keysets:

AS-11B Standard keyset with handfree speaker-phone feature.

AS-11E LCD display added to the standard features.

AS-11BV Voice Message Service added to the standard features.

AS-11EV LCD display and Voice Message Service added to the standard features.

AS-11 series are controlled by the included CPU, Intel 8051, and the operations are directed by the data from KSU, SKP-308H.

The related main system is SKP-308H system but this model can operate well connected to the other systems; SKP-308, SKP-816, SKP-816H, SKP-36HX, and SKP-56/120H. For installation to the SKP-56/120H system, the special board, MSLC2 is required.

There are so many buttons for one-touch feature accomplishment; 3 DTS, 8 DSS, 1 FAX buttons, 12 dial buttons, 6 one-touch Dial buttons, 10 feature buttons, and LCD viewing angle control knob. FUNC/DND, TRSF/ALM, PAGE, SPK, MSG, RD, FLASH, HOLD, VOLUME-UP, VOLUME-DOWN buttons are all the feature buttons.

AS-11 series provide the audible and visual services with the various tones and ring-tones, and LED's and LCD.

30 DTS/DSS buttons and 8 feature buttons except for volume control buttons are equipped with LED's, RED or RED/GREEN. The first 12 DTS/DSS buttons include the dual LED's; Green LED indicates the outside line is used by the user and Red LED says the line is used by the other subscriber.

AS-11 series are largely composed of Main set, Handset, Line Cord, Handset cord, and Wall-mount/Desk Bracket, based on the structure.

Main set is divided into two parts; Top Housing Ass'y and Base Plate, which are jointed with four screws. Top Housing Ass'y consists of Top Plate and some plastics, LCD Module, Mike Ass'y, Speaker Ass'y, Key B'd Ass'y, and Control B'd Ass'y, which are jointed with screws and the connection between LCD Module and Control B'd Ass'y and the connection between Key B'd Ass'y and Control B'd Ass'y are made with the flexible cables and the connectors.

Handset is composed of two dynamic units, one modular jack ass'y, two cover plastics, and some screws. The dynamic units are transducers from the physical voice signals to the electrical signals or from the electrical signals to the physical voice signals.

Line Cord connects the Main set to the KSU through the terminal block and MDF and cables.

Handset Cord connects the handset to the Main set, which is curled with four (4) wires.

Wall-mount/Desk Bracket is a support to Main set for a better view. The standard installation provides the desk type and the reverse installation provides the wall-mount type.

The assembly diagram is already provided in "Assembly & Disassembly" chapter.

AS-11 series are composed of plastics and the sensitive semiconductor devices, so it should be installed and maintained carefully; No Fire, No Shock, No Water, No Air-Tight, and No Electrical/Magnetic Shock. Otherwise, the set may be damaged critically.

AS-11 series are electrically composed of the following circuits:

- CPU and its peripherals
- Data Communication circuit
- Key Scanning circuit
- LED driving circuit
- 1 line 16 character LCD and its interface with viewing angle control (Set Option)
- Handset Hook On/Off Detector
- Ring Tone Generator with digital volume control
- Key Confirmation Tone Generator
- Speech Hybrid circuit
- Network, four by four cross-points
- Handset Interface circuit with digital volume control
- Speaker-phone circuit
- Speaker Driving circuit with digital volume control
- Voice Message Service circuit (Set Option)
- External Speaker interface circuit (Individual)
- Power Regulators (DC-DC converter)

AS-11 series keyset is connected to the Key Service Unit through the line modular jack (6P/6C Top). The modular jack has three pair signal lines. One of them consists of pin 3 and pin 4, which is assigned to the speech path and the system ground is fed through the line for the keyset power. The other consists of pin 2 and pin 5, which is assigned to the data path and the system 30 volt DC is fed through the line for the keyset power. The last one consists of pin 1 and pin 6 which is the individual external paging path. The first and second pathes are connected to KSU through MDF and cables, and the last pair may be connected to the external small-capacity speaker AMP if necessary.

CPU & PERIPHERALS

Intel 8051 is used as CPU of which major features are as follows:

- 8-bit CPU
- On-chip Oscillator
- 4K bytes of Program Memory
- 128 bytes of Data Memory
- 21 Special Function Registers
- 32 I/O lines
- 64K address space for external Data Memory
- 64K address space for external Program Memory
- Two 16-bit Timer/Counters
- A five-source interrupt structure with two priority levels
- A full duplex serial port
- Bit addressability for Boolean processing

For this product, any external memory is not used. The detail features may be referred from Intel data book but it must not be necessary to support the keyset.

The system clock is provided with 11.059MHz crystal, and its machine cycle is 1.085 micro-second for one machine cycle requires 12 system clocks. For good oscillation with little distortion, the crystal by-pass capacitors are determined to 47 pico-farad in their capacitances.

To prevent from radiating EMI [Electro-Magnetic Interference], the 5-volt power is fed to CPU in series with EMI filter, CFI 103M which is internally composed of two small-inductance ferrite beads and 10 nano-farad capacitor. The filter blocks CPU noise from transmission, which reduces the radiation of the noise.

To protect CPU from a electrical shock or trap, a reset circuitry may be required, which should be composed of the level detector and the watch-dog circuit.

A level detector may monitor the power variation of CPU and resets and protect CPU and the internal memory if the power is detected out of range. The level detector equipped in AS-30 series is composed of a capacitor, two signal diodes, and some passive components. The reference voltage is provided with two diodes (D1, D2) by their forward voltage drops. The devices determine the threshold voltage about 4.0 volt and the reset signal, high state over 3.0 volt activates CPU restart if 5 volt power varies under the threshold voltage. Otherwise, the comparator output sustains Low. The threshold voltage is determined as following equations:

$$\text{Threshold Voltage} = ((R2 + R3)/R3) * V_{ref}$$

Intel 8051 has high-active reset structure and the level detector is designed to generate High signal during the abnormal power supply. The level detector is activated to reset CPU when the power on/off or any power variation during operation.

A watch-dog circuit monitors CPU operation, and generates the reset signal when it detects the mis-operation of CPU. The detection can be accomplished with the watch-dog clear signal. During operation, CPU provides the periodic clear signal to the watch-dog circuit but the signal will be stuck to low or high state when the program drops to a trap or CPU perceives a mis-operation, for example, the absence of the data from the system.

The watch-dog circuit is composed of a comparator (U2B), five switching diodes, and some passive devices. The circuit is a pulse generator, regardless of the input signal of the clear signal. Let's see the operation of the pulse generator. The comparator has two feedback path; the positive and negative feedback. The positive feedback enhances the operation of the comparator and it provides the difference between the high threshold reference and the low threshold reference which are the levels of the non-inverting terminal. The negative feedback is a charging and discharging path to the capacitor, C25.

Pulse generation is accomplished as follows;

Suppose that the initial potential of the capacitor, C25 is zero. The level of the non-inverting terminal is higher than the inverting terminal level, so the comparator output is high state pulled with the resistor, R11. The level of the non-inverting terminal becomes the high threshold reference for the output is high. In this case, the capacitor, C25 is charged with the high output through the negative feedback resistor, R10. The charging operation is characterized with the resistance of R10 and the capacitance of C25. The inverting level increases owing to the charging operation and the level becomes higher than the non-inverting terminal later. Then, the output becomes low and the non-inverting level varies to low threshold reference and the operation of the capacitor changes to discharging. This charging and discharging operation repeats and the output generates the pulse signals. As described, Intel 8051 has the high-active reset structure and the High output can be applied to reset CPU. The duration of high output is called as Reset Time and the duration of low output is called as Watch-dog Time. The starting high duration is especially called as Power On Reset Time.

Power-on-reset time, watch-dog time, and reset time can be calculated like as following:

Firstly, let me explain the operation of the non-inverting terminal. The terminal provides the reference to the comparator and the level varies according to the output. The non-inverting level during high output is High Threshold Reference and the level during low output is Low Threshold Reference.

$$\begin{aligned} V(TH) &= R8 / ((R7 // R9) + R8) * VCC \\ &= 3.33_V \text{ if } VCC \text{ is five volts.} \end{aligned}$$

$$\begin{aligned} V(TL) &= (R8 // R9) / (R7 + (R8 // R9)) * VCC \\ &= 1.66_V \text{ if } VCC \text{ is five volts.} \end{aligned}$$

Based on the threshold level, the durations are determined with charging or dis-charging time of the capacitor. Power-On-Reset time can be defined as charging time from ground to the high threshold level, Watch-dog time can be defined as discharging time from the high threshold level to the low threshold time, and Reset time can be defined as charging time from the low threshold time to the high threshold time.

Power-on-reset time can be calculated; the charging time to the high threshold level without any initial charge. It can be expressed as the following equation.

$$\text{High Threshold} = VCC (1 - e^{** (-t/(C25R10))}) = 3.33$$

$$(1 - e^{** (-t/(C25R10))}) = 0.666 \quad VCC = 5V$$

$$-t/(C25R10) = -1.0966, \quad C25R10 = 0.3$$

$$t = 0.329$$

Power-On-Reset Time is 329ms.

Watch-dog time can be calculated; the discharging duration from the high threshold level to the low threshold level of the inverting terminal.

$$V(TH) e^{** (-t/(C25R10))} = V(TL)$$

$$e^{** (-t/(C25R10))} = V(TL)/V(TH)$$

$$t = 0.209$$

Watch-dog Time is 209ms.

Reset time also can be calculated; the charging duration from the low threshold level to the high threshold level of the inverting terminal.

$$VCC - (VCC - V(TL))e^{** (-t/(C25R10))} = V(TH)$$

$$e^{** (-t/(C25R10))} = (VCC - V(TH))/(VCC - V(TL)) = 0.5$$

$$t = 0.208$$

Reset Time is 208ms.

Regardless of the clear signal input, the circuit generates pulse train continuously; Starting High Pulse (Power-On-Reset), Low state (Watch-dog), High state (Reset), Low state, etc.

As described, any abnormal state results in stopping the clear signal input, and the circuit generates the reset signal to restart CPU.

At normal state, CPU generates the clear signal continuously. The clear signal is coupled by the capacitor, C24 and the diodes, D3 and D4 are clipping the lower level than the charged level at the capacitor, C25. As above, the clear signal charges the capacitor to maintain the capacitor level higher than the low threshold level. Otherwise, the capacitor potential will become down to the low threshold level and it results in generating the reset signal (High state). The diode D5 will dis-charge all the potential of the charged capacitor when power failure and enhance the power-on-reset characteristics.

The outputs of the level detector and the watch-dog circuit are simply connected to produce the OR logics. Any high state of them should be transferred to the reset terminal of CPU for it has the high-active reset interface. So, OR logic is necessary to combine two outputs.

The pull-up resistors result from the open-collector outputs of the comparator and one serial resistor and one blocking diode make the OR logic. Owing to the interface, the high output of the level detector will be fully transferred to CPU reset terminal and the high output of the watch-dog circuit will be converted to 3.5V of which level is enough to reset CPU.

Let's see the reset operation. When the keyset is connected to working KSU, the power is fed to keyset. Then the logic power, 5 volt will rise and the level detector will generate a short power-on-reset pulse according to the power rising time. In addition to this, the watch-dog circuit generate 329ms high pulse to reset CPU. The power-on-reset signal protects CPU from the power transition and guarantees the initial time for the peripheral devices, especially crystal, which stabilizes all the operation of the peripheral devices before CPU runs.

After power-on-reset time, CPU starts to run and it checks buttons. It detects whether any one of buttons is stuck or not. It is very important because all the buttons are the tools for the man-machine communications and key-sticking disturbs the right detection of key-pressing (button pressing).

If CPU perceives a key-sticking during checking buttons, CPU stops generating the watch-dog clear signal and drives the HOLD LED to be flickered. Stopping the watch-dog clear signal causes the reset signal to CPU as described, and the previous initialing procedure repeats.

After checking the buttons, CPU starts to receive and transmit its data to KSU and it requests to be registered in the system. But, CPU may causes the reset and drives SPK LED emitted if it can not receive any data from KSU. Any data absence may cause the reset with SPK LED emission.

In addition to these, the watch-dog circuit may perceive any program-sticking and the level detector perceive any power variation and it generates the reset signal at that case.

CPU & its peripherals control all the circuits in the keyset and any little fault at this part may be the critical failure of the keyset.

DATA COMMUNICATION CIRCUIT

The data communications between KSU and keyset are accomplished through the second pair of line cord and the data are made by CPU internal timer and transmitted via [DATA TX] port. The data from KSU are received through [DATA RX] port. The signalling method is asynchronous anmd serial. Each bit duration is 3mS.

RECEIVING DATA

1 Start bit	Low state
3 Network ID	MSB first, network control data
8 Data bits	MSB first
8 Data bits	MSB first
2 Waiting bits	High state

The data from KSU are inverted in the de-modulation circuit and the RX data are composed of 22 bits including two waiting bits as above. After receiving KSU data, the keyset sends its data to KSU.

TRANSMIT DATA

1 Start bit	High state
1 Parity bit	Even parity check
7 Data bits	MSB first
2 Waiting bits	Low state

~~Totally, one data monitoring between KSU and keyset requires 33 bits, that is, 99mS.~~

The data transmitted are amplified with the data TX OP-AMP and modulated to the pulse-differential signals through the resistor (4.7K ohm) and the capacitor (100 nF). The time constant is determined to 0.47mS based on the values of the capacitor and resistor owing to the bit duration of 3mS. And, the received data are the differential-modulated signals and they are recovered/de-modulated with the comparator. The comparator circuit is a inverting latched flip-flop and its noise margin is determined by the value of the passive devices attached to the non-inverting input, R29 and R30. The noise margin is set to ± 0.8 volt based on the reference voltage fed by the voltage divider. The comparator operates with 12 volt power and its saturated output swings up to 11 volts which is not adequate to apply to CPU port. So, the output level of the comparator is divided with two resistors, R31 and R32.

As described, the pulse-differential modulation are adopted to the data communications between KSU and keyset, which generates the high peak signals and they may leaks to the speech path when the loop distance between KSU and keyset is long. The leakage may cause a ticking noise at the speech path it may disturb the user.

It is very difficult to remove the ticking noise and a special low-pass filter for the speech path may be required.

KEY SCANNING CIRCUIT

There are so many buttons in the keyset; 3 DTS, 8 DSS, 1 FAX buttons, 12 dial buttons, 6 one-touch dial and 10 feature buttons, totally 40 buttons. All of these buttons should be monitored by CPU whether a button is pressed or not.

Genrally, there are two kinds of key-scanning methods; Static scanning and Dynamic scanning. The static scanning required the individual detector and the application circuit is very simple. It does not generate any noise but it requires the same number of detectors.

Dynamic scanning requires small controls and it provides the possibility to scan the large amount of buttons. It is economic to the system which has the large amount of buttons but it may produce the scanning noise which may interfere the digital logics or the speech path if it is not prevented. The keyset has so many buttons and the scanning circuit is composed with the dynamic scanning method.

All of the buttons are composed to a matrix for the dynamic scanning and the scanning signals are fed to the row and they are detected through the columns. With the row scanning signals and the column detection data, CPU can perceive which button is pressed. Refer to the key board circuit diagram.

The matrix of buttons is 8 by 8 and one of them is applied to determine the keyset kinds. It is prepared for the independent sales at the same place but there will be no opportunity to divide the keyset kinds. Ignore it. The rows of the matrix are composed of the latch, 74HCT373 U1 on key board and the columns of the matrix are copmposed of eight signal diodes which are driven with the pull-up resistors.

CPU scans the buttons periodically as follows;

CPU latches the row scanning data to the buffer and the bit for scanning row is set to low and the others are set to high. That is, it uses the low-active scanning method. After activating the first row, CPU reads the column data through the signal diodes. If any one of the first row buttons is pressed, one or two of the column data will be read as Low. Otherwise, all the bits of the column data will be read as high.

As above, the other rows can be scanned.

The button contacts are made of carbon and each contact has some hundred ohm resistance based on the procedure of PCB manufacture. And, the detection level of CPU bus is 0.8V at maximum. To meet the detection condition, the reading path is composed of the carbon contact, diode, and pull-up resistor. Here, the pull-up resistor effects largely. The pull-up resistor determines the current through the path and the forward voltage drop of the diode can be determined based on the current. And, the voltage drop on the carbon contact is also determined based on the current. The voltage drops will reduce as the current reduces and the voltage drops will increase as the current increases. Therefore, to stabilize the detecting opertaion, reducing the current is essential. To reduce the current, the resistance of pull-up resistor should be selected to the large value.

But, a large pull-up resistor may disturb to drive the related devices for the pull-up resistor is connected to the data bus and it effects all the operation of the bus. Large pull-up resistor will reduce the pan-out/pan-in characteristics and it may cause the critical error for CPU to drive or read the devices.

Based on the above two conditions, the pull-up resistors are selected to 47K ohms in their resistances.

LED DRIVING CIRCUIT

LED driving circuit consists of one row driver, one column driver, and 26 LED's. 3 DTS (Direct Trunk Selection) buttons, 1 FAX button have the dual color LED's for indications. The green LED indicates that you are using the line and the red LED indicates that the other is using the line. The 8 DSS buttons, 6 one-touch dial buttons and 8 feature buttons have single color LED's, RED.

There are two kinds of methods to drive LED's, Static and Dynamic. Static driving method needs the same number of drivers and it generates a little noise. Each driving line is simply controlled, High or Low. But, it has a shortcoming; it requires the same number of control lines to drive LED's and it is not adequate to drive a lot of LED's. To drive lots of LED's, the dynamic driving method is applied.

Dynamic driving method requires a little control lines and it is simple to assign the control circuit but it requires some complicate controls and generates some noise which should be considered during design.

The keyset applies the dynamic driving method to drive LED's owing to the quantity of LED's. 74HCT373, U2 is assigned to the row driver and UCN5801A is assigned to the column driver. The column driver may drive eight LED's at the same time if necessary, then a high current driver should be applied. UCN5801A, U3 has the internal Darlington TR arrays and that is the reason to apply the chip to the column driver.

All of LED's are composed of matrix, eight rows and eight columns and driving LED's are mainly up to column driving.

Each column is activated at every 8 ms. During the first one milli-second, the first column is activated and the other columns are disabled. During the next one milli-second, the second column is activated and the other columns are disabled. As above, each column is periodically activated at every 8 ms. To activate the column, the related data bit should be set to high and the other bits should be low, and the latch enable signal of the column driver should be controlled, because the driver has the darlington TR arrays and they operate as inverters and the low state activates the related column line.

Column driving works continuously and the related row data can be driven based on the LED data from KSU. During column driving, any high signal at the row may activate the related LED ON. The row driver, 74HCT373 has two control signals and eight data interfaces. One of control signals is for latching the data and the other is for output enable signal.

As described, each LED has the 1/8 duty cycle and Turn-on means that one milli-second ON during 8 ms. That looks the continuous ON by the human eye.

To drive LED is manipulated at the CPU program based on the internal timer.

All of LED's are Surface Mounted Devices and they are very sensitive to any mechanical shock. At the condition of set assembly, the keyset is designed for resisting the shock but you should take care of the key board during dis-assembly or repairing.

The row driver (U2 74HCT373), the column driver (U3 UCN5801A), and LED's are installed on the key board.

LCD INTERFACE WITH VIEWING ANGLE CONTROL

One line sixteen (16) character LCD is equipped in AS-11E and AS-11EV models, which is controlled by one controller and driver. The LCD controller is interfaced with CPU and the operation of controller is indicated by CPU. LCD (Liquid Crystal Display) equipped with its controller and driver is usually called as LCD module.

To approach LCD module is divided to two operations, reading and writing. Reading operations enable to detect the status of the controller and writing operations enable to send the instructions and data to the controller. During writing operations, [LCDRS] determines the instructions or data; Low state of [LCDRS] indicates the instruction and the high state of [LCDRS] indicate the display data.

[LCDRW] control signal determines the reading or writing operations. Before normal operations, LCD should be initialized as follows:

[LCD Initializing Routine]

```
Power On
Wait more than 15mS
Function Set
    Specify the number of display lines, data bits, and
    character fonts. They should not be changed afterwards.
Wait more than 4.1mS
Function Set (repeat)
Wait more than 100uS
Function Set (repeat)
Function Set (repeat)
Display Off
Display On
Entry Mode Set
    Specify the display data entry mode; Increment/Decrement
    or Display Shift.
End of initialization
```

After initializing the LCD module, CPU can send the display data to the module. The LCD module has 14 pin interface connector of which pin assignments are as follows:

[LCD Connector Pin Assignment]

Pin 1	GND
Pin 2	VCC
Pin 3	VLCD
Pin 4	LCDRS
Pin 5	LCDRW
Pin 6	LCD EN
Pin 7 - 14	D0 - D7

CPU can write and read the data through the connector. One is prepared on the control board and the other is prepared on the key board, and they are connected through the LCD cable, flexible one.

The data assignments to control the LCD module are as follows:

X : don't care

CONTROLS										FUNCTION DESCRIPTION
RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	0	1	Clear Display (1.64mS)
0	0	0	0	0	0	0	0	1	X	Clear Display & Return Home (1.64mS)
0	0	0	0	0	0	0	1	I/D	S	Entry Mode Set (40uS) I/D : Increment/Decrement S : Accompanies Display Shift
0	0	0	0	0	0	1	D	C	B	Display On/Off Control (40uS) D : Display On/Off C : Cursor On/Off B : Blink On/Off
0	0	0	0	0	1	S/C	R/L	X	X	Cursor or Display Shift (40uS) S/C : Display or Cursor Shift R/L : Shift Right or Left
0	0	0	0	1	DL	N	F	X	X	Function Set (40uS) DL : 8 or 4 bit data N : 1 or 2 line F : 5 * 10 or 5 * 7 Dots
0	0	0	1	-	-	-	-	-	-	Set CG RAM address (40uS)
0	0	1	-	-	-	-	-	-	-	Set DD RAM address (40uS)
0	1	BF	-	-	-	-	-	-	-	Read Busy Flag & ADDR (0uS)
1	0	-	-	-	-	-	-	-	-	Write data to CG or DD RAM (40uS)
1	1	-	-	-	-	-	-	-	-	Read data from CG or DD RAM (40uS)

The previous table for the detail controls is not required to maintain or repair the keyset but to understand the LCD operation may helpful.

To control the LCD module requires three control signals; one is for chip selection [LCD EN], the other is for indicating instruction/data [LCDRS], and the last is for reading/writing indications [LCDRW]. Two of them, [LCDRS] and [LCDRW] are multiplexed with the control signals for key scanning and LED driving.

The third pin of the connector is for adjusting the viewing angle, and the level is usually set to one level. But the keyset has the control knob for this. The slide volume may adjust the viewing angle and it is useful to users. Because, there are so many practices to install the keyset and to cover all the angle of display is very difficult. Therefore, this control knob enables the user to adjust the viewing angle of LCD. Two resistors and one variable resistor enable to adjust the level of the VLCD pin.

HANDSET HOOK ON/OFF DETECTOR

A micro-switch (Single Pole Single Contact, S1) is prepared to detect the hook status of handset. When hook-on, the switch contact is open and CPU may read High status through Port 2.0 owing to the pull-up resistor, R12. When hook-off the switch contact is closed and CPU may read Low status because one of the switch terminals is connected to ground of keyset.

CPU approaches the port 2.0 periodically and it serves the related feature based on the instructions from KSU.

Compared with single line telephones, handset hook switch is only one switch for the status in keyset because all of the operations of keyset are controlled by CPU. The read status may be sent to KSU through data-com circuit and CPU may receive the relating data from KSU, which are the instructions for keyset operations.

RING-TONE GENERATOR WITH VOLUME CONTROL

Ring-tone signal is generated through CPU port [RING] by program of which On/Off is also controlled through the port. CPU can generate some mixed single frequencies [pulse train] and they are used as ring-tone signal. By the aid of program generation, four kinds of ring-tone signals are provided, which are selected by user-programming. The variety of the ring-tone is determined by the mixed rate of the different frequencies.

The generated ring-tone signals are fed to SPEAKER VOLUME CONTROL circuit and the level is manipulated there. The volume is simply adjusted; Voltage dividing with three analog switches. The level varies 8 steps by control of three analog switches, of which control signals are [SPK_GAIN1], [SPK_GAIN2], and [SPK_GAIN3].

[Ring-Tone Volume Control]

SPK_GAIN3	SPK_GAIN2	SPK_GAIN1	Volume Status
L	L	L	Minimum Volume
L	L	H	2nd Volume
L	H	L	3rd Volume
L	H	H	4th Volume
H	L	L	5th Volume
H	L	H	6th Volume
H	H	L	7th Volume
H	H	H	Maximum Volume

This volume control circuit is also used for the speaker-phone RX volume control and the control signals are independently manipulated by CPU according to the status. During ringing and the specific programming, any volume up/down button may increase/decrease the value of ring buffer and the value of ring buffer is used to set the volume during ringing. For speaker-phone RX volume, the other buffer is prepared and controlled independently by CPU. Ring-tone signals are also fed to the external speaker interface, which is described later.

KEY CONFIRMATION TONE GENERATOR

If one of dial buttons is pressed, a confirmation tone is heard; that is called as ~~Key Confirmation Tone~~ or ~~Key-Tone~~ by an abbreviated form. CPU generates 1000 Hz single frequency signal and it bursts during 100ms immediately after a valid Dial Key is pressed.

By the aid of program generation, the interface circuit is very simple; some passive components.

When Key Confirmation Tone is served, the volume control level is fixed to the minimum level and the tone path is selected to speaker or handset. During speaker-phone, the control signal [SPK CS] is activated to Low, which selects also the key-tone path to speaker. The path to handset is always connected but it is very difficult to hear the tone from handset when it is in the cradle. The path to handset enables the user to hear the tone through handset.

The level of the generated tone is adjusted with the resistors which are attached to the port 1.6. After the level adjustment, the serial capacitor prevents any DC coupling and the signals are divided to handset or speaker. To handset, the signals are fed to handset RX amplifier through the input resistor. To speaker, the path is controlled with the transistor C1009Y for the logic inversion. Connected at the switch, the signals may be fed to speaker driver LM386.

~~Every pressing any dial button may activate the key confirmation signal during 100ms.~~ The signals will not serve when the other buttons are pressed and it is the design specification, which is more useful.

SPEECH HYBRID CIRCUIT

The keyset is equipped with the ~~speech hybrid circuit~~ to accommodate mixing or dividing the speech signals to/from TX and RX. The speech signals on the system network or the line is the mixed forms of TX and RX signals and they should be divided. And, the speech signals in the keyset should be mixed to send. The speech hybrid circuit works the feature.

The circuit is divided to two parts; ~~hybrid TX amplifier~~ and ~~hybrid RX amplifier~~. Handset TX or micro-phone signals are connected to the hybrid TX amplifier through the network. And, the amplified signals are transferred to KSU via the power-isolated transformer, 5692.

The speech signals received through the transformer are fed to the hybrid RX amplifier and the output signals are connected to handset RX or speaker-phone circuit through the network. ~~Each direction signals are restricted to voice band, from 300Hz to 3400Hz.~~

To mix the transmitted and received signals generates the feedback signals which are usually called as ~~Sidetone~~. The speech hybrid circuit determines the side-tone level according to the trunk loop length. The TX signals are fed to the inverting and non-inverting terminals of the RX OP-AMP to compensate and reduce the level through the related passive components.

NETWORK

The keyset is equipped with the network which is composed of four by four matrix. CD22100 is the network chip and it has the 4 by 4 matrix cross-points. All of the connections for speech signals are accomplished with the network and the chip is the most important for the speech transmission. The chip has some control ports to connect/dis-connect the internal cross-points. One is assigned for chip selection [NETWORK EN] and it is used for latching the data to the data interface of the chip. The chip selection signal is active-High. The next is assigned for the instruction for connecting/dis-connecting the selected cross-point according to the status. High state connects the cross-point and the low state dis-connects the cross-point. D7 is used for the connection instruction operated with the chip selection. To select the cross-points can be accomplished with data bits D0 to D3 operated with the chip selecting signal. These 4 data bits select one of the sixteen (16) cross-points.

The pathes of speech signals are connected to the network as follows:

<u>Row Connections</u>	HANDSET TX SPK TX (Speaker-phone TX) HYBRID RX VMS SIGNAL (VMS reproducing signal)
<u>Column Connections</u>	HYBRID TX HANDSET RX SPK RX (Speaker-phone RX) VMS RECORD (VMS recording signal)

Each row and column may be connected or dis-connected by the data written from CPU as described above.

The cases of calls in keyset are considered; Handset Speech, Handset Mute, Speaker-phone Speech, Speaker-phone Mute, VMS Recording, VMS Reproducing to Handset, VMS Reproducing to Speaker, and VMS Reproducing to KSU.

The connections of the call states are as follows:

[Network Controls for the Call Cases]	
Call Case	Required connection
Handset Speech	HANDSET TX to HYBRID TX HANDSET RX to HYBRID RX
Handset Mute	HANDSET RX to HYBRID RX
Speaker-phone Speech	SPK TX to HYBRID TX SPK RX to HYBRID RX
Speaker-phone Mute	by [SPK MUTE] signal
VMS Recording	HANDSET TX to VMS RECORD
VMS Reproducing to Handset	HANDSET RX to VMS SIGNAL
VMS Reproducing to Speaker	SPK RX to VMS SIGNAL
VMS Reproducing to KSU	HYBRID TX to VMS SIGNAL

The previous table informs the necessary connecting points and all the cross-points except for the informed points should not be connected. Otherwise, it may result in the critical error to speech transmission.

The other combinations of network become the critical faults of the operations. The speaker-phone and VMS operations require the additional controls which will be described later.

HANDSET INTERFACE CIRCUIT

The keyset is equipped with a handset of which transducers are dynamic units. The physical voice signal is transduced to the electrical signal through the moving coil of the TX dynamic unit and the received electrical signal is transduced to the physical voice signal through the RX dynamic unit. And, the units are connected to the handset interface circuit on the control board through the handset modular ass'y, handset cord, and handset modular jack. The dynamic units, handset modular ass'y, and the mechanical parts are assembled to Handset Ass'y. Handset cord is a curl cord of which standard length is 300mm. Sometimes, the special one of which length is 450mm may be supplied according to the buyer request.

Four (4) pin wires are required to connect handset to the main set. One pair (modular pin 1 and 4) is allocated to TX path, from the TX dynamic unit to the handset TX interface. The other (modular pin 2 and 3) is allocated to RX path, from the handset RX interface to the RX dynamic unit.

The electrical signal generated from the TX dynamic unit is a weak signal and it requires the large amplification without noise. The TX signal is fed to the handset TX interface through the serial coupling capacitor. The dynamic unit does not require any DC voltage compared with condenser micro-phone.

The handset TX interface is composed of the small signal amplifier of which gain is determined with the rate of the input and the feedback resistors. The amplifier is the negative feedback OP-AMP and the input signal is fed to the inverting terminal of which reference DC voltage is fed through the non-inverting terminal. The input coupling capacitor decides the low cutoff frequency with the input resistor and the feedback capacitor decides the high cutoff frequency with the feedback resistor. The frequency characteristics are very important because the line for the tele-communications has its own pass-band.

The reference DC voltage is got with dividing the 12 volt and used as the signal reference. The ~~zener diode connected to the output protects the network from any over-voltage~~ for the network path is set from GND to 5 volts. The output of the TX interface is fed to network and it may be connected to the other interface there if necessary.

The received signals fed from the network are connected to the handset RX volume control circuit. The ~~handset RX volume control circuit~~ is composed of two analog switches and some passive devices. The principle is very simple. Switch-on decreases the input resistance of the handset RX amplifier and results in increasing the gain. Based on two control ports, [H/S_GAIN1] and [H/S_GAIN2], the handset RX volume varies by four steps. The volume can be manipulated with the volume up/down button touch during handset speech case. ~~The varistor connected between the terminals of OP-AMP protects the user from any acoustic shock.~~ The signal reference DC is fed through the non-inverting terminal and the gain of the amplifier is determined with the rate of the input and the feedback resistors, which may vary according to the handset RX volume control.

The input signals are fed to the inverting terminal and the key confirmation tone signals are also fed to the terminal.

The output is connected to the handset RX dynamic unit through the serial resistor and the coupling capacitor.

For handset interface, RC5532, dual OP-AMP chip is used for the two small signal amplifiers, of which driving power is 12 volts.

SPEAKER-PHONE CIRCUIT

All the keyset are equipped with ~~speaker-phone facility~~ basically. Compared with handset speech, speaker-phone can be accomplished with ~~short-time half duplex~~. Otherwise, a howling may disturb the communications because the microphone and the speaker have the capability to cover the large area compared with handset speech. Therefore, a automatic half-duplex switch device is essential to the speaker-phone facility.

MC34018 supplied by Motorola is the main device to switch RX/TX automatically. The main feature of the chip is switching TX/RX based on the level of which changeover speed is also adjusted with the external passive devices. The chip requires so many external devices and all of them have their meanings. For the detail operations and the applications, refer to the data sheet supplied by Motorola.

The chip is supplied with 5 volt power and it has the chip selector activated by the low state. So, the chip selection signal should be activated for the speaker-phone operation. The 5 volt power is supplied through the RC filter to prevent the switching noise.

For the transmitting transducer, a condenser micro-phone is applied, which requires the driving DC voltage. The micro-phone is assembled with the wire harness and connected through 2 pin connector. The condenser micro-phone has the polarity.

The generated electrical signal is fed to the analog switch which is prepared to control speaker-phone mute. The control signal is one of CPU ports, [SPK MUTE] and the low state dis-connects the path and results in the mute facility of speaker-phone.

The signals through the analog switch, U9D, flow to the speaker-phone chip and are amplified there. The amplified signals are attenuated and fed to the internal comparator to decide switching. If the switch is selected to TX, then the signals may be connected to the other interface through the network.

The received signals from the network are fed to the chip and attenuated and compared with the transmit signals for switching. If the switch is selected to RX the signals are fed to the speaker volume control circuit.

To adjust the switching facility is very difficult because there are so many call cases and so many loop cases. The switching mechanism is very simple but to set the feature to operate well at any case is tiresome. The speaker-phone facility may be improved by trial and error based on the field reports. Your practical and honest reports may be helpful to us.

SPEAKER DRIVER WITH VOLUME CONTROL

The product uses 0.3W, 8 ohm loud speaker and uses LM386 as the speaker driver. The driver is supplied with 5 volt power through the RC filter to prevent the driving noise from interfering the other circuits. The output terminating resistor and capacitor may block any unpredicted oscillation. The speaker driver input is fed from the speaker volume control circuit.

The speaker volume control circuit is composed of three analog switches and some passive devices. As described, the volume control circuit is used to adjust the speaker-phone RX volume as well as the ring-tone volume. The volume levels according to the control signals are same with the table described at the description section of the ring-tone generator.

The input of the volume control circuit is connected to the speaker-phone RX and ring-tone generator, and the node is also connected to the external speaker interface circuit.

One of the key confirmation tone outputs is connected to the speaker driver directly.

The volume control circuit operates for the speaker-phone as well as ring-tone signals but the control logics are manipulated respectively.

VOICE MESSAGE SERVICE CIRCUIT

This circuit is equipped only in the VMS models, AS-11BV and AS-11EV. It is for the voice message feature; Voice Message Sending feature and Voice Alarm feature.

The circuit prepares 60 second voice recording/reproducing feature which can be divided to five blocks. The first three blocks are assigned to the voice alarm features and the fourth block is for the intercom message and the last is for the outside message. The user can select the ring alarm or voice alarm if he wants to be served with the alarm features and the maximum three voice alarms can be available.

The intercom message can operate when there is a intercom call during out-of-place. And, the outside message can be automatically activated only at the attendant port when the outside call is arriving based on user-programming.

For the voice message service, the circuit consists mainly of VMS processor KS5917 and four 41256 DRAM's provided by Samsung Electronics Semiconductor division. The processor can record an analog signal to RAM by delta modulation, and may reproduce the recorded signal. The sampling rate may be selected, but 16 Kbps sampling rate is chosen in the product. And, the number of recording phrases may be also selected up to 16 but 8 phrases can be selected in application and 5 phrases are assigned.

For signal recording, handset should be used. [HANDSET TX] signal can be connected to the processor through the network, amplified, sampled, and stored to DRAM memories. During developing the product, the condenser micro-phone was considered as recording source but the environmental noise disturbs the clean recording. So, the recording source was changed to handset.

For signal reproducing, the stored data are got from DRAM, converted to the analog signal, amplified, and transmitted to network. In the network, the signal may be switched to [HYBRID TX] for sending to KSU, intercom voice message or outside voice message. And switched to [HANDSET RX] or [SPK RX] for self reproducing or voice alarm.

74HCT373 is applied to control the processor reset, recording/reproducing selection, starting, stopping, phrase selection, and VMS existence check.

EXTERNAL SPEAKER INTERFACE CIRCUIT

The product has the External Speaker interface for individual loud bell service. The circuit is designed to accomodate the individual paging feature but the current system program can not serve the paging feature.

The interface is composed of one analog switch for ON/OFF control, one OP-AMP for signal amplification, and one transformer for power isolation. The signal pair is connected to the pin 1 and 6 of line modular jack. The signal comes from the input of the speaker volume control.

A external speaker with amplifier should be connected if necessary. The external speaker with amplifier is not supplied by Samsung Electronics. It may be got in market.

The interface can be controlled with user programming.

POWER REGULATORS

The product uses 5 volt and 12 volt power for the operations. The main power is about 24 volts supplied from KSU through the center-tapped terminals of data and speech transformers. The reference potential is fed through the speech path and the high potential is fed through the data path. The power is converted to 5 volt and 12 volt with DC-DC convertors.

For 5 volt regulation, Si8201L is applied, which is the hybrid component including 5 volt switching regulator. The electrical characteristics are as follows:

Input Voltage	45V max
Output Volatge	5.0V typ
Output Current	400mA max

And, 78L12 is applied to 12 volt regulator. That is the linear regulator of which input voltage is 35V max. Zener diode 1N4752A is also applied for over-voltage protection.

5 volt power is applied to all the logic parts and some speech circuitry, the network, the speaker-phone circuit, and the speaker driver. 12 volt power is applied to handset speech circuit, speech hybrid circuit, and the data communication circuit.

2. VOLTAGE CHART

This section describes the voltage informations on the detail parts in the system and the keyset, based on the features.

A. SYSTEM VOLTAGE CHART

FUNCTION	COMP. (PIN)	BOARD	STATUS	DESCRIPTIONS
Main DC Power	P3 (1)	Power	24V - 30V	Unregulated DC Power of which value varies according to AC input & load.
	ZD1 (-)	Power	6.2V	DC regulating reference.
Battery Charge	U4 (2)	Power	6.2V	Charge control reference
	U4 (1)	Power	Bat. or GND	Charge path control signal. Low state connects charging path. Threshold = 28.0 V (factory adjusting)
Battery Dis-charge	U4 (5)	Power	5.75V or 6.65V	Discharge control reference.
	U4 (7)	Power	Bat. or GND	Discharge path control signal. Low state connects discharging path. TH = 24.6V, TL = 21.4V
12V DC Power	U5 (1)	Power	24V - 30V	Unregulated DC Power is fed to input.
	U5 (3)	Power	12.0V	12V DC output. This 12V is supplied to all the necessary parts.
24V DC Power for Base board	U8 (1)	Power	24V - 30V	Unregulated DC Power is fed to input.
	U8 (3)	Power	24.0V	24V DC output. Mainly used to drive relays on base board.
5V DC Power for Base board	U6 (5)	Power	24V - 30V	Unregulated DC Power is fed to input.
	U6 (1)	Power	5.0V	5V DC output. Supplied to all the necessary parts including control logics on base board.

FUNCTION	COMP. (PIN)	BOARD	STATUS	DESCRIPTIONS
Reset operation	U1 (9)	Base	Low	During operation.
			High	CPU Reset
	U1 (8)	Base	H $\leftrightarrow$ L	Watch-dog clear signal. During operation.
			H or L	System Trap
Data Bus operation	U1 (39)	Base	H $\leftrightarrow$ L	Address & Data 0
	U1 (38)	Base	H $\leftrightarrow$ L	Address & Data 1
	U1 (37)	Base	H $\leftrightarrow$ L	Address & Data 2
	U1 (36)	Base	H $\leftrightarrow$ L	Address & Data 3
	U1 (35)	Base	H $\leftrightarrow$ L	Address & Data 4
	U1 (34)	Base	H $\leftrightarrow$ L	Address & Data 5
	U1 (33)	Base	H $\leftrightarrow$ L	Address & Data 6
	U1 (32)	Base	H $\leftrightarrow$ L	Address & Data 7
Data Bus operation	U5 (18)	Base	H $\leftrightarrow$ L	Data Bus bit 0
	U5 (17)	Base	H $\leftrightarrow$ L	Data Bus bit 1
	U5 (16)	Base	H $\leftrightarrow$ L	Data Bus bit 2
	U5 (15)	Base	H $\leftrightarrow$ L	Data Bus bit 3
	U5 (14)	Base	H $\leftrightarrow$ L	Data Bus bit 4
	U5 (13)	Base	H $\leftrightarrow$ L	Data Bus bit 5
	U5 (12)	Base	H $\leftrightarrow$ L	Data Bus bit 6
	U5 (11)	Base	H $\leftrightarrow$ L	Data Bus bit 7
Address Bus operation	U1 (21)	Base	H $\leftrightarrow$ L	Address Bus bit 8
	U1 (22)	Base	H $\leftrightarrow$ L	Address Bus bit 9
	U1 (23)	Base	H $\leftrightarrow$ L	Address Bus bit 10
	U1 (24)	Base	H $\leftrightarrow$ L	Address Bus bit 11

FUNCTION	COMP. (PIN)	BOARD	STATUS	DESCRIPTIONS
Address Bus Operation (continued)	U1 (25)	Base	H $\leftrightarrow$ L	Address Bus bit 12
	U1 (26)	Base	H $\leftrightarrow$ L	Address Bus bit 13
	U1 (27)	Base	H $\leftrightarrow$ L	Address Bus bit 14
	U1 (28)	Base	H $\leftrightarrow$ L	Address Bus bit 15
	U2 (2)	Base	H $\leftrightarrow$ L	Address Bus bit 0
	U2 (5)	Base	H $\leftrightarrow$ L	Address Bus bit 1
	U2 (6)	Base	H $\leftrightarrow$ L	Address Bus bit 2
	U2 (9)	Base	H $\leftrightarrow$ L	Address Bus bit 3
	U2 (12)	Base	H $\leftrightarrow$ L	Address Bus bit 4
	U2 (15)	Base	H $\leftrightarrow$ L	Address Bus bit 5
	U2 (16)	Base	H $\leftrightarrow$ L	Address Bus bit 6
	U2 (19)	Base	H $\leftrightarrow$ L	Address Bus bit 7
CPU additional control signals	U1 (29)	Base	H $\leftrightarrow$ L	Program Send Enable. Active-Low.
	U1 (30)	Base	H $\leftrightarrow$ L	Address Latch Enable. Active per machine cycle
	U1 (16)	Base	H $\leftrightarrow$ L	Write Enable signal. Active-low only during writing cycle.
	U1 (17)	Base	H $\leftrightarrow$ L	Read Enable signal. Active-low only during reading cycle.
	U1 (31)	Base	Low	Effective Address. Always low state.
	U1 (18)	Base	Sinewave	System clock. 11.059MHz

FUNCTION	COMP. (PIN)	BOARD	STATUS		DESCRIPTIONS
			STANDBY	OPERATION	
Real Time Clock	U6 (2)	Base	High	Low	RTC /CS0
	U6 (15)	Base	High	High	RTC CS1. Low only when power off.
	U6 (18)	Base	High	High	RTC power
	U6 (9)	Base	Low	Low	RTC GND
	U6 (8)	Base	H $\leftrightarrow$ L	H $\leftrightarrow$ L	CPU /RD
	U6 (10)	Base	H $\leftrightarrow$ L	H $\leftrightarrow$ L	CPU /WR
	U6 (4)	Base	H $\leftrightarrow$ L	H $\leftrightarrow$ L	Address Bit 0
	U6 (5)	Base	H $\leftrightarrow$ L	H $\leftrightarrow$ L	Address Bit 1
	U6 (6)	Base	H $\leftrightarrow$ L	H $\leftrightarrow$ L	Address Bit 2
	U6 (7)	Base	H $\leftrightarrow$ L	H $\leftrightarrow$ L	Address Bit 3
	U6 (14)	Base	H $\leftrightarrow$ L	H $\leftrightarrow$ L	Data Bit 0
	U6 (13)	Base	H $\leftrightarrow$ L	H $\leftrightarrow$ L	Data Bit 1
	U6 (12)	Base	H $\leftrightarrow$ L	H $\leftrightarrow$ L	Data Bit 2
	U6 (11)	Base	H $\leftrightarrow$ L	H $\leftrightarrow$ L	Data Bit 3
	U6 (17)	Base	Sinewave	Sinewave	32768Hz
First Station Hook Off (Keyset)	U12 (19)	Base	H $\leftrightarrow$ L	H $\leftrightarrow$ L	TX data
	U12 (11)	Base	H $\leftrightarrow$ L	H $\leftrightarrow$ L	TX data LE
	U13 (2)	Base	H $\leftrightarrow$ L	H $\leftrightarrow$ L	RX data
	U13 (1,19)	Base	H $\leftrightarrow$ L	H $\leftrightarrow$ L	RX data /RD
	U7 (18)	Base	Low	H $\leftrightarrow$ L	Network ST
	U8 (11)	Base	High	H $\leftrightarrow$ L	Network data latch enable
	U7 (38,5,22,23,4,24,25,2)	Base	Keep the status	changed	Network address & control

FUNCTION	COMP. (PIN)	BOARD	STATUS		DESCRIPTIONS
			STANDBY	OPERATION	
8th Station (SLT) Hook Off	U18 (13)	Base	High	High	SLT Loop Relay Drive
	U16 (17)	Base	High	Low	SLT Hook Det
	D15 (+)	Base	GND	Sinewave	Dial Tone
	U44 (1)	Base	24V	24V	SLT DC Feed
	U44 (6)	Base	GND	GND	SLT GND
	U44 (7)	Base	5V	5V	SLC-01 Power
	U7 (18)	Base	Low	H $\leftrightarrow$ L	Network ST
	U8 (11)	Base	High	H $\leftrightarrow$ L	Network data latch enable
	U7 (38,5, 22,23,4,24, 25,2)	Base	Keep the status	changed	Network address & control
	U9 (7)	Base	Low	H $\leftrightarrow$ L	Tone Network Strobe
8th Station (SLT) Dialing, Dial Pulse	U16 (2)	Base	Low	H $\leftrightarrow$ L	SLT Hook Detector
8th Station (SLT) Dialing, DTMF	U16 (2)	Base	Low	Low	SLT Hook Detector
	D15 (+)	Base	GND	DTMF	Speech path
	U23 or U24 or U25 (15)	Base	Low	High	Valid DTMF Detection
	U21 & U24 & U25 (7)	Base	Sinewave	Sinewave	3579545Hz. MFR clock
Ringing at 8th Station (SLT)	K8 (8)	Base	80V, 20Hz	80V, 20Hz	Ring Signal
	K8 (4)	Base	DC	80V, 20Hz	Ring Signal
	P3 (8)	Power	80V, 20Hz	80V, 20Hz	Ring Source

FUNCTION	COMP. (PIN)	BOARD	STATUS		DESCRIPTIONS
			STANDBY	OPERATION	
1st Trunk Access	U15 (2)	Base	High	Low	Trunk Loop Detector
	U17 (20)	Base	High	Low	Trunk Relay Driving
	D17 (+)	Base	GND	Sinewave	Dial Tone
1st Trunk Dialing, Dial Pulse	U15 (2)	Base	Low	H $\leftrightarrow$ L	Trunk Loop Detector
	U17 (20)	Base	Low	H $\leftrightarrow$ L	Trunk Relay Driving
	U17 (2)	Base	Low	H $\leftrightarrow$ L	Trunk Relay Driver LE
1st Trunk Dialing, DTMF	U15 (2)	Base	Low	Low	Trunk Loop Detector
	U17 (20)	Base	Low	Low	Trunk Relay Driving
	U17 (2)	Base	Low	Low	Trunk Relay Driver LE
	D17 (+)	Base	GND	Sinewave	DTMF
1st Trunk Ringing	U15 (2)	Base	High	H $\leftrightarrow$ L	Trunk Loop Detector
	U17 (20)	Base	High	High	Trunk Relay Driving
	U49 (1 & 2)	Base	Low	Sinewave	Ring Signal

FUNCTION	COMP. (PIN)	BOARD	STATUS		DESCRIPTIONS
			STANDBY	OPERATION	
Auto-Redial thru 1st Trunk	U17 (20)	Base	High	Low	
				H $\leftrightarrow$ L	Pulse dialing
	U15 (2)	Base	High	Low	
				H $\leftrightarrow$ L	Pulse dialing
	U22 (9)	Base	Low	High	Valid detect.
Door-phone Access	D38 (+)	Base	GND	Speech	Speech path
	U19 (9)	Base	High	H $\Rightarrow$ L $\Rightarrow$ H	Door Lock
Door-phone Call	D38 (+)	Base	GND	GND	Speech path
	U19 (9)	Base	High	High	Door Lock
	U15 (8)	Base	High	Low	While Door button is pressed
Internal Music	U26 (14)	Base	Melody	Melody	Int. Music
	U53 (1)	Base	Melody	Melody	Driver output
External Music	D32 (+)	Base	Music	Music	Ext. Music
	U53 (1)	Base	Music	Music	Driver output
External Page	D36 (+)	Base	GND	Speech	Speech path

B. KEYSET VOLTAGE CHART

FUNCTION	COMP. (PIN)	BOARD	STATUS	DESCRIPTIONS
5V DC Power	D10, ZD10 (-), C101 (+)	Control	19V - 30V	Unregulated DC Power supplied from KSU
	U11 (1), C102 (+)	Control	5.0V	5V DC Power output
12V DC Power	C103 (+)	Control	19V - 30V	Unregulated DC Power supplied from KSU
	U12 (0), C104 (+)	Control	12.0V	12V DC Power output
Common Control	U1 (40)	Control	5.0V	CPU Power
	U1 (20)	Control	GND	CPU GND
	U1 (31)	Control	High	Effective Address
	U1 (18, 19)	Control	H $\leftrightarrow$ L	System Clock. 11.059MHz sinewave.
	U1 (29)	Control	High	Program Send Enable
	U1 (30)	Control	H $\leftrightarrow$ L	Address Latch Enable
	U1 (39)	Control	H $\leftrightarrow$ L	Data Bus Bit 0
	U1 (38)	Control	H $\leftrightarrow$ L	Data Bus Bit 1
	U1 (37)	Control	H $\leftrightarrow$ L	Data Bus Bit 2
	U1 (36)	Control	H $\leftrightarrow$ L	Data Bus Bit 3
	U1 (35)	Control	H $\leftrightarrow$ L	Data Bus Bit 4
	U1 (34)	Control	H $\leftrightarrow$ L	Data Bus Bit 5
	U1 (33)	Control	H $\leftrightarrow$ L	Data Bus Bit 6
	U1 (32)	Control	H $\leftrightarrow$ L	Data Bus Bit 7
Reset Operation	U1 (9)	Control	High	CPU Reset. Normal Low.
	U2 (1)	Control	High	VCC, out-of-range. Otherwise, VCC in range.
	U2 (7)	Control	High	Watch-dog activated. Otherwise, set operates.
	U1 (22)	Control	H $\leftrightarrow$ L	Watch-dog Clear. Otherwise, set trapped

FUNCTION	COMP. (PIN)	BOARD	STATUS	DESCRIPTIONS	
Data-Com Operation	U1 (1)	Control	H ⇄ L	Data TX to KSU	
	U1 (2)	Control	H ⇄ L	Data RX to KSU	
	U3 (1)	Control	H ⇄ L	Data TX to KSU	
	U3 (7)	Control	H ⇄ L	Data RX to KSU	
	D7 (+)	Control	Differ- ential signals	Modulated signals. TX & RX mixed.	
FUNCTION	COMP. (PIN)	BOARD	STATUS		DESCRIPTIONS
			STANDBY	OPERATION	
Key Scanning	U1 (20)	Key B'd	5.0V	5.0V	U1 VCC
	U1 (10)	Key B'd	GND	GND	U1 GND
	U1 (11)	Key B'd	H ⇄ L	H ⇄ L	Minute Duty
	U1 (1)	Key B'd	H ⇄ L	H ⇄ L	Large Duty
	U1 (2)	Key B'd	H ⇄ L	H ⇄ L	1st Row
	U1 (5)	Key B'd	H ⇄ L	H ⇄ L	2nd Row
	U1 (6)	Key B'd	H ⇄ L	H ⇄ L	3rd Row
	U1 (9)	Key B'd	H ⇄ L	H ⇄ L	4th Row
	U1 (12)	Key B'd	H ⇄ L	H ⇄ L	5th Row
	U1 (15)	Key B'd	H ⇄ L	H ⇄ L	6th Row
	U1 (16)	Key B'd	H ⇄ L	H ⇄ L	7th Row
	U1 (19)	Key B'd	H ⇄ L	H ⇄ L	8th Row
	D1 (-)	Key B'd	Float	as row	1st Column
	D2, D3, D4, D5, D6, D7, D8 (-)	Key B'd	Float	Float	2nd, 3rd, 4th, 5th, 6th, 7th, 8th Column

FUNCTION	COMP. (PIN)	BOARD	STATUS		DESCRIPTIONS
			STANDBY	OPERATION	
LED Driving (1st DTS/DSS Green LED Turn-On, others are Off)	U2 (20)	Key B'd	High	High	U2 VCC Power
	U2 (10)	Key B'd	GND	GND	U2 GND
	U2 (11)	Key B'd	H $\leftrightarrow$ L	H $\leftrightarrow$ L	U2 Latch En
	U2 (1)	Key B'd	H $\leftrightarrow$ L	H $\leftrightarrow$ L	U2 Output En
	U3 (21)	Key B'd	High	High	U3 VCC Power
	U3 (11)	Key B'd	GND	GND	U3 GND
	U3 (2)	Key B'd	H $\leftrightarrow$ L	H $\leftrightarrow$ L	U3 Latch En
	U3 (22)	Key B'd	GND	GND	U3 Output En
	U2 (2)	Key B'd	Low or Float	H $\leftrightarrow$ L, Float	1st LED Row
	U2 (5, 6, 9, 12, 15, 16, 19)	Key B'd	Low or Float	Low or Float	2nd, 3rd, 4th, 5th, 6th, 7th, 8th LED row
	U3 (13, 14, 15, 16, 17, 18, 19, 20)	Key B'd	Float $\leftrightarrow$ L	Float $\leftrightarrow$ L	1st, 2nd, 3rd, 4th, 5th, 6th, 7th, 8th, LED Column
LCD Display	P4 (1)	Control	GND	GND	LCM GND
	P4 (2)	Control	5V	5V	LCM VCC
	P4 (3)	Control	DC	DC	VLCD. Level varies as Slide Volume.
	P4 (4)	Control	H $\leftrightarrow$ L	H $\leftrightarrow$ L	Command/Data
	P4 (5)	Control	H $\leftrightarrow$ L	H $\leftrightarrow$ L	Read/Write
	P4 (6)	Control	H $\leftrightarrow$ L	H $\leftrightarrow$ L	Chip Select
	P4 (7, 8, 9, 10, 11, 12, 13, 14)	Control	H $\leftrightarrow$ L	H $\leftrightarrow$ L	Data Bus Bit0 thru Bit7

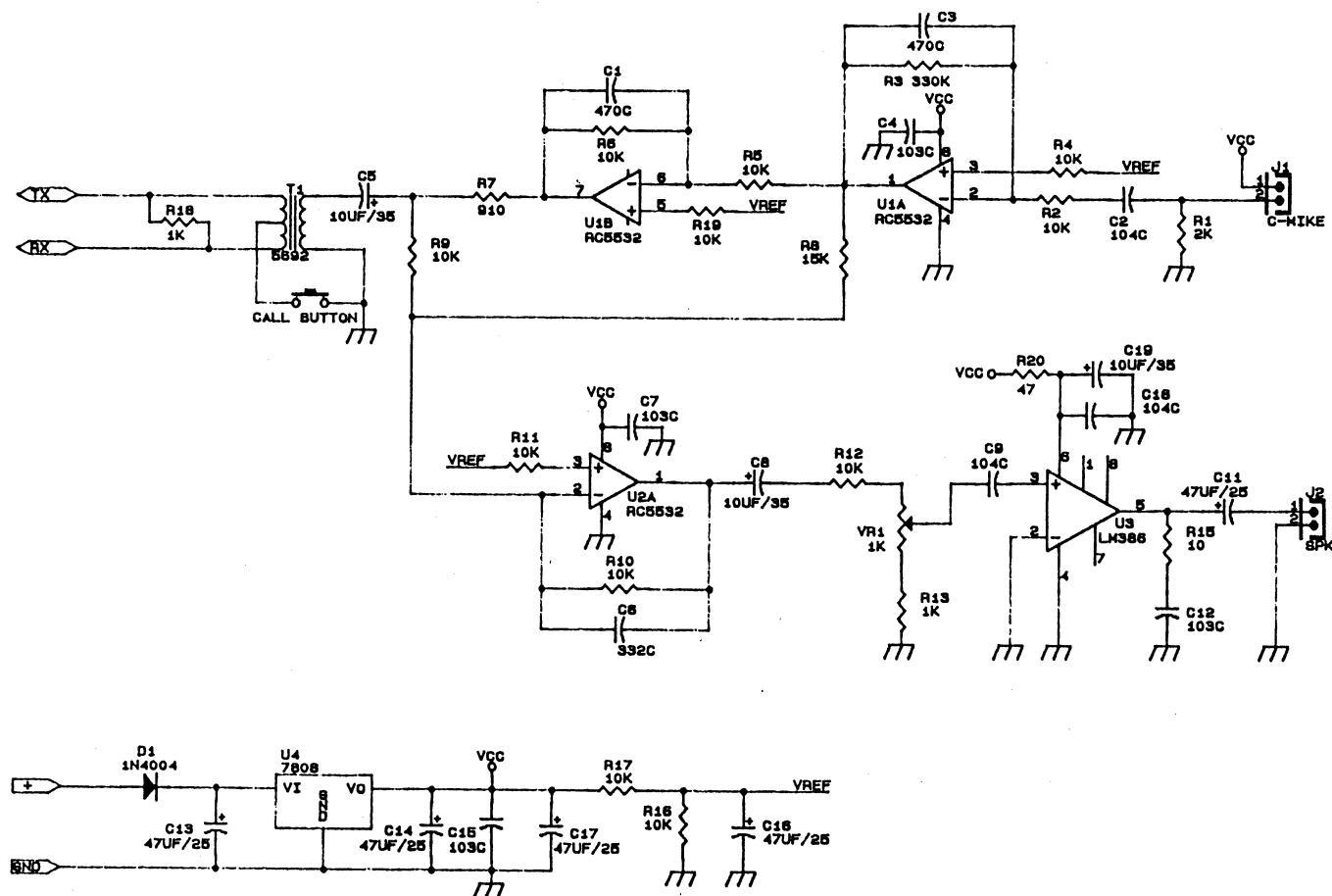
FUNCTION	COMP. (PIN)	BOARD	STATUS		DESCRIPTIONS
			STANDBY	OPERATION	
Handset Speech	U1 (21)	Control	High	Low	Hook Detector
	U4 (7)	Control	H $\leftrightarrow$ L	H $\leftrightarrow$ L	Network LE
	U6 (1)	Control	DC	DC + Speech	Handset TX OP-AMP output
	U4 (9)	Control	DC	DC + Speech	Handset TX
	U4 (15)	Control	Float	DC + Speech	Hybrid TX
	U5 (1)	Control	DC	DC + Speech	Hybrid TX OP-AMP output
	U5 (7)	Control	DC	DC + Speech	Hybrid RX OP-AMP output
	U4 (12)	Control	Float	DC + Speech	Hybrid RX
	U4 (14)	Control	DC	DC + Speech	Handset RX
	U6 (7)	Control	DC	DC + Speech	Handset RX OP-AMP output
Speaker-phone	U10 (18)	Control	High	Low	U10 Chip Sel
	U4 (7)	Control	H $\leftrightarrow$ L	H $\leftrightarrow$ L	Network LE
	U9 (6)	Control	Low	High	Mike Mute CTL
	U4 (1)	Control	GND	DC + Speech	SPK-phone TX
	U4 (15)	Control	Float	DC + Speech	Hybrid TX
	U4 (12)	Control	Float	DC + Speech	Hybrid RX
	U4 (10)	Control	DC	DC + Speech	SPK-phone RX
	U8 (5)	Control	GND	Speech	SPK Driving

FUNCTION	COMP. (PIN)	BOARD	STATUS		DESCRIPTIONS
			STANDBY	OPERATION	
Key Confirmation Tone - Dial Button pressed	U1 (7)	Control	High	H $\leftrightarrow$ L	Key Tone Src
	U6 (7)	Control	DC	DC + Tone	H/S RX Drive
	U8 (5)	Control	GND	Key Tone	SPK Drive in SPK-phone
Ringing	U1 (8)	Control	High	H $\leftrightarrow$ L	Ring Source
	U9 (2)	Control	DC	DC + Ring	SPK Vol. CTL
	U8 (5)	Control	GND	Ring Tone	SPK Drive
Loud Bell	U1 (8)	Control	High	H $\leftrightarrow$ L	Ring Source
	U9 (2)	Control	DC	DC + Ring	SPK Vol. CTL
	U7 (2)	Control	Float	DC + Ring	Ext SPK Input
	U13 (7)	Control	DC	DC + Ring	Ext SPK Output
VMS Recording	U14 (2)	Control	Low	Low	VMS Reset
	U14 (5)	Control	--	High	VMS Rec/Rep
	U14 (6)	Control	Low	H $\Rightarrow$ L	To Start
	U14 (9)	Control	Low	H $\Rightarrow$ L	To Stop
	U4 (13)	Control	Float	DC + Speech	VMS Recording signal fr H/S
	U15 (30)	Control	DC	DC + Speech	VMS A/D input
VMS Reproducing	U14 (2)	Control	Low	Low	VMS Reset
	U14 (5)	Control	--	Low	VMS Rec/Rep
	U14 (6)	Control	Low	H $\Rightarrow$ L	To Start
	U14 (9)	Control	Low	H $\Rightarrow$ L	To Stop
	U15 (31)	Control	DC	DC + Speech	VMS D/A output
	U4 (11)	Control	DC	DC + Speech	VMS Reproduce to Network

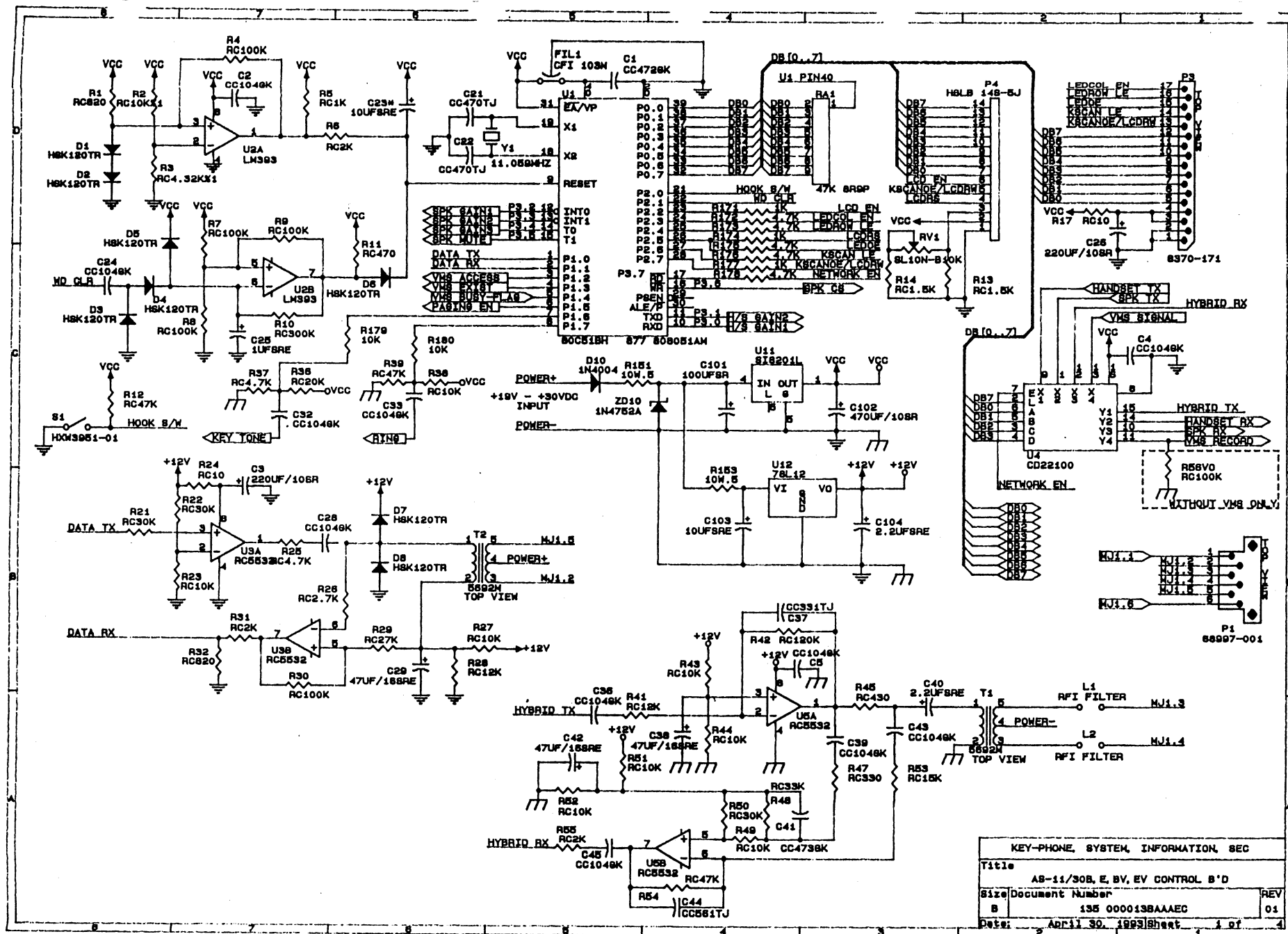
3. C I R C U I T D I A G R A M

C O N T E N T S

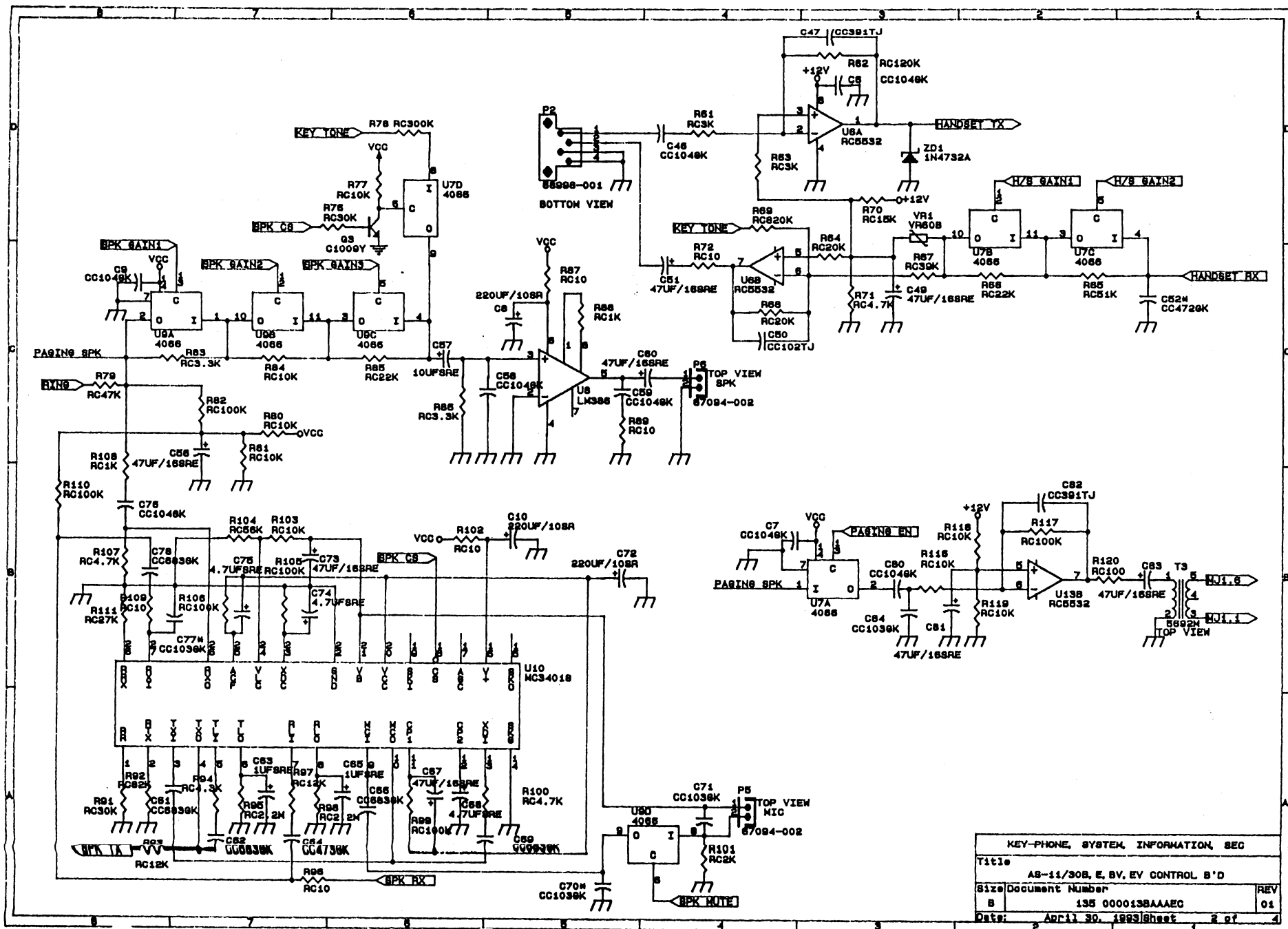
Base Board & Power Board Circuit Diagram	145
Door-phone Circuit Diagram	147
AS-11/30B, E, BV, EV Control Board Circuit Diagram A ...	148
AS-11/30B, E, BV, EV Control Board Circuit Diagram B ...	149
AS-11/30B, E, BV, EV Control Board Circuit Diagram C ...	150
AS-11/30B, E, BV, EV Key Board Circuit Diagram	151



KEY-PHONE, SYSTEM, INFORMATION, SEC		
Title		
DOOR-PHONE CIRCUITRY FOR SAMSUNG KTS		
Size	Document Number	REV
B	650 240624HAAAEC	01
Date: September 14, 1992 Sheet 1 of 1		



KEY-PHONE SYSTEM INFORMATION, SEC			
Title	AS-11/30B, E, BV, EV CONTROL S'D		
Size/Document Number	135 0000138AAEC		
REV	01		
Date:	APR 130, 1993	Sheet	1 of 4



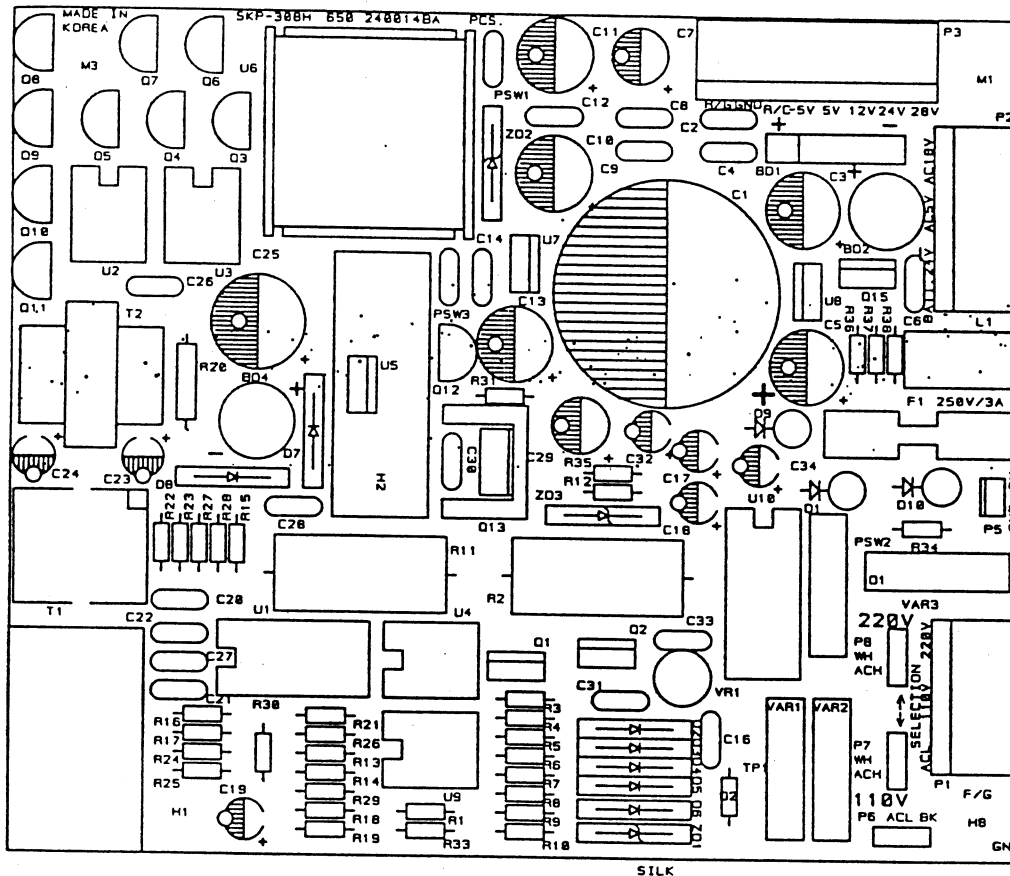
KEY-PHONE SYSTEM INFORMATION, SEC			
Title			
AS-11/308, E, BV, EV CONTROL S'D			
Size/Document Number			
B	135 0000138AAAEC	REV	01
Date: April 30, 1993 Sheet 2 of 4			

4 . C O M P O N E N T L A Y O U T

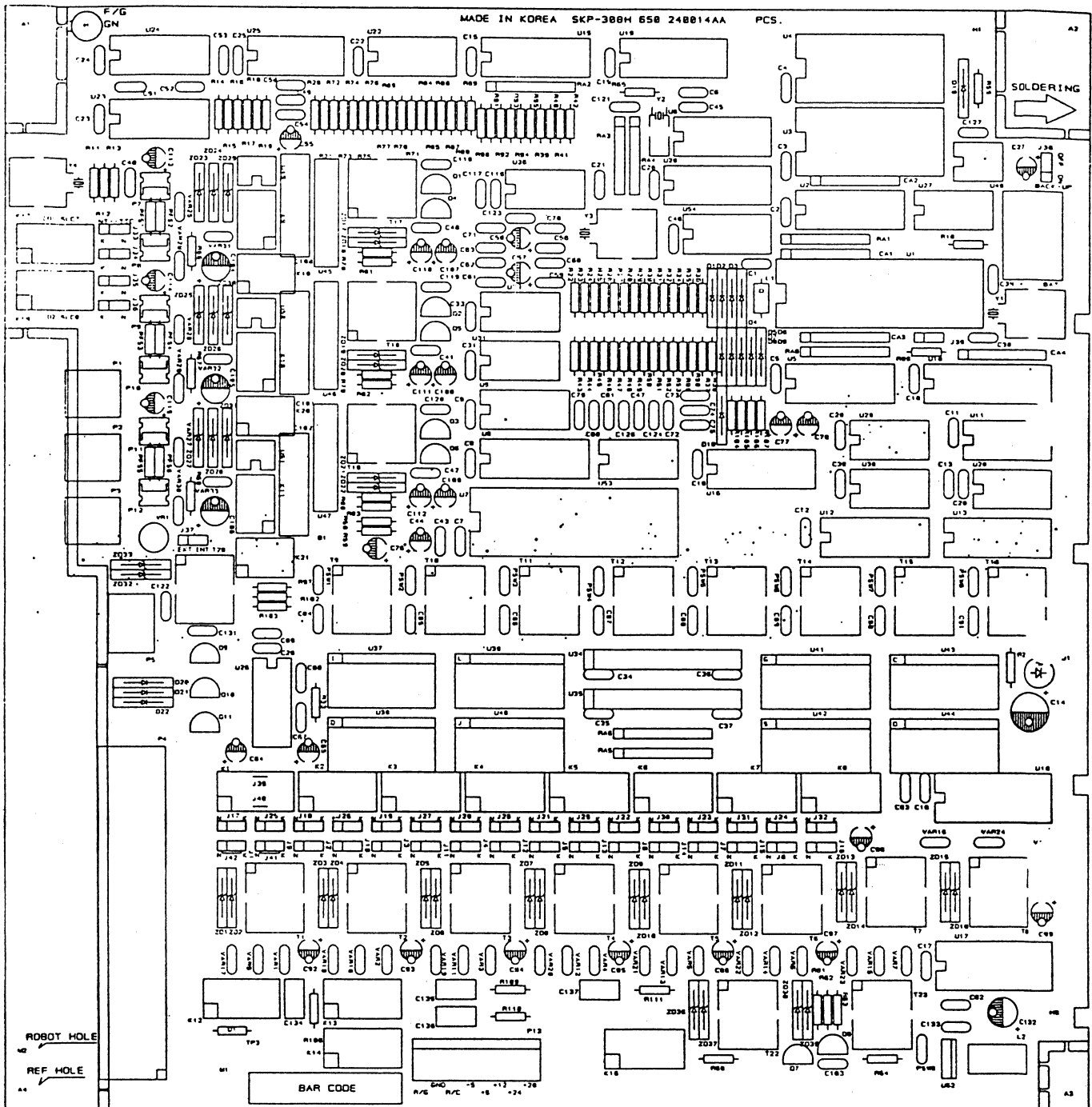
C O N T E N T S

Power Supply Board Component Layout	155
Base Board Component Layout	156
AS-11/30BV, EV Control Board C/S Component Layout	157
AS-11/30BV, EV Control Board S/S Component Layout	158
AS-11/30B, E Control Board C/S Component Layout	159
AS-11/30B, E Control Board S/S Component Layout	160
AS-11B, E, BV, EV Key Board C/S Component Layout	161
AS-11B, E, BV, EV Key Board S/S Component Layout	162

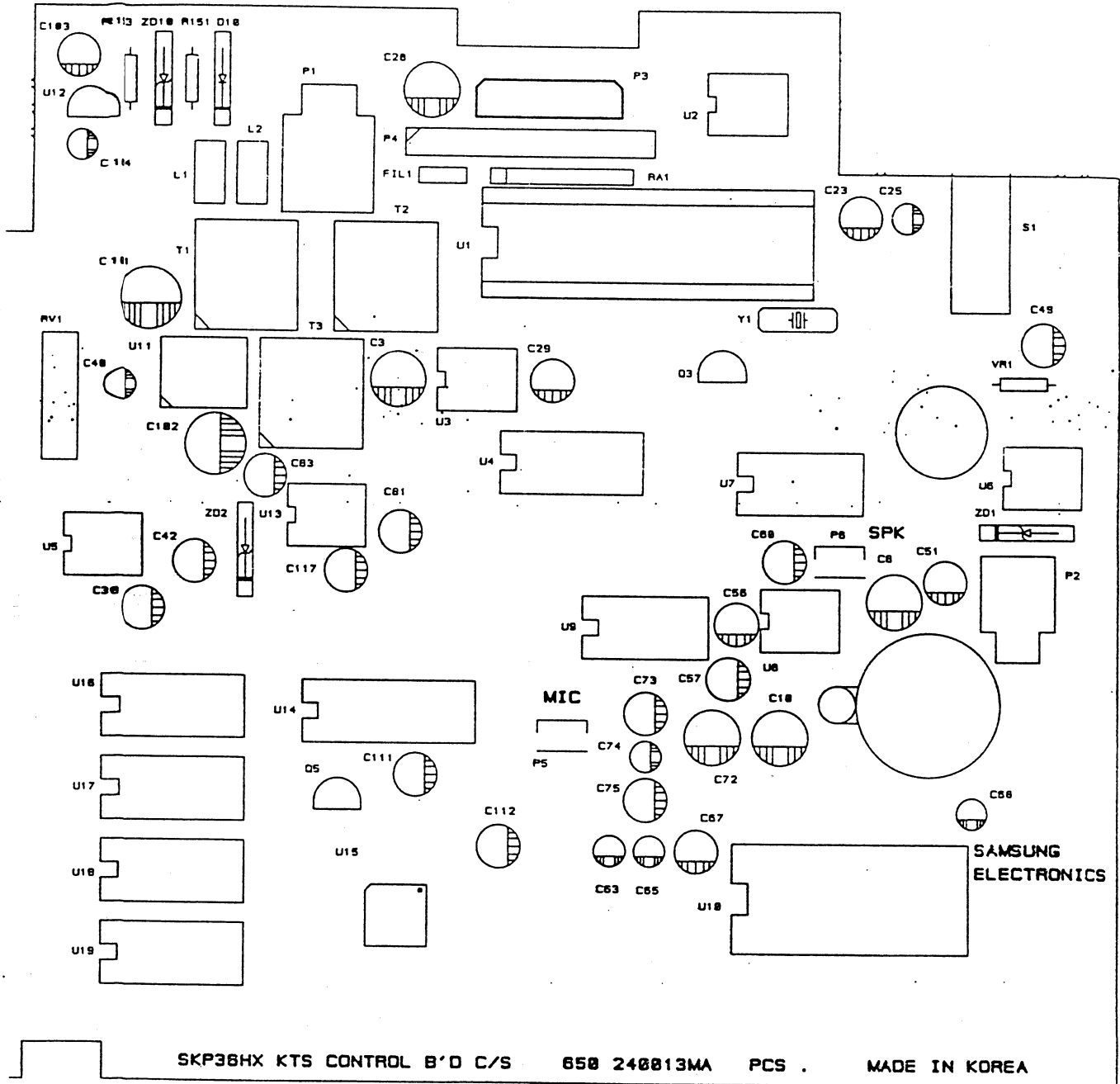
Power Supply Board Component Layout



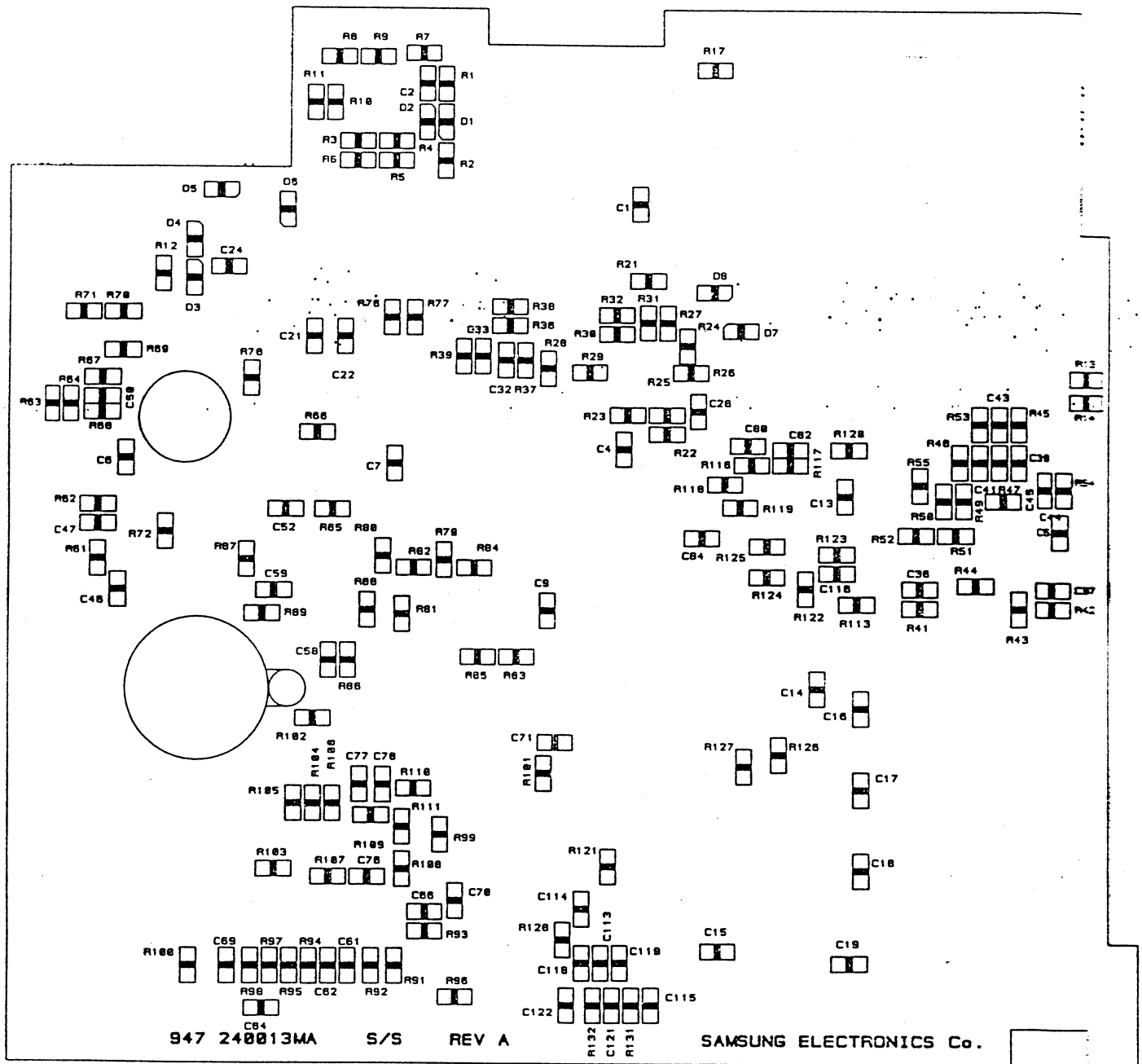
Base Board Component Layout



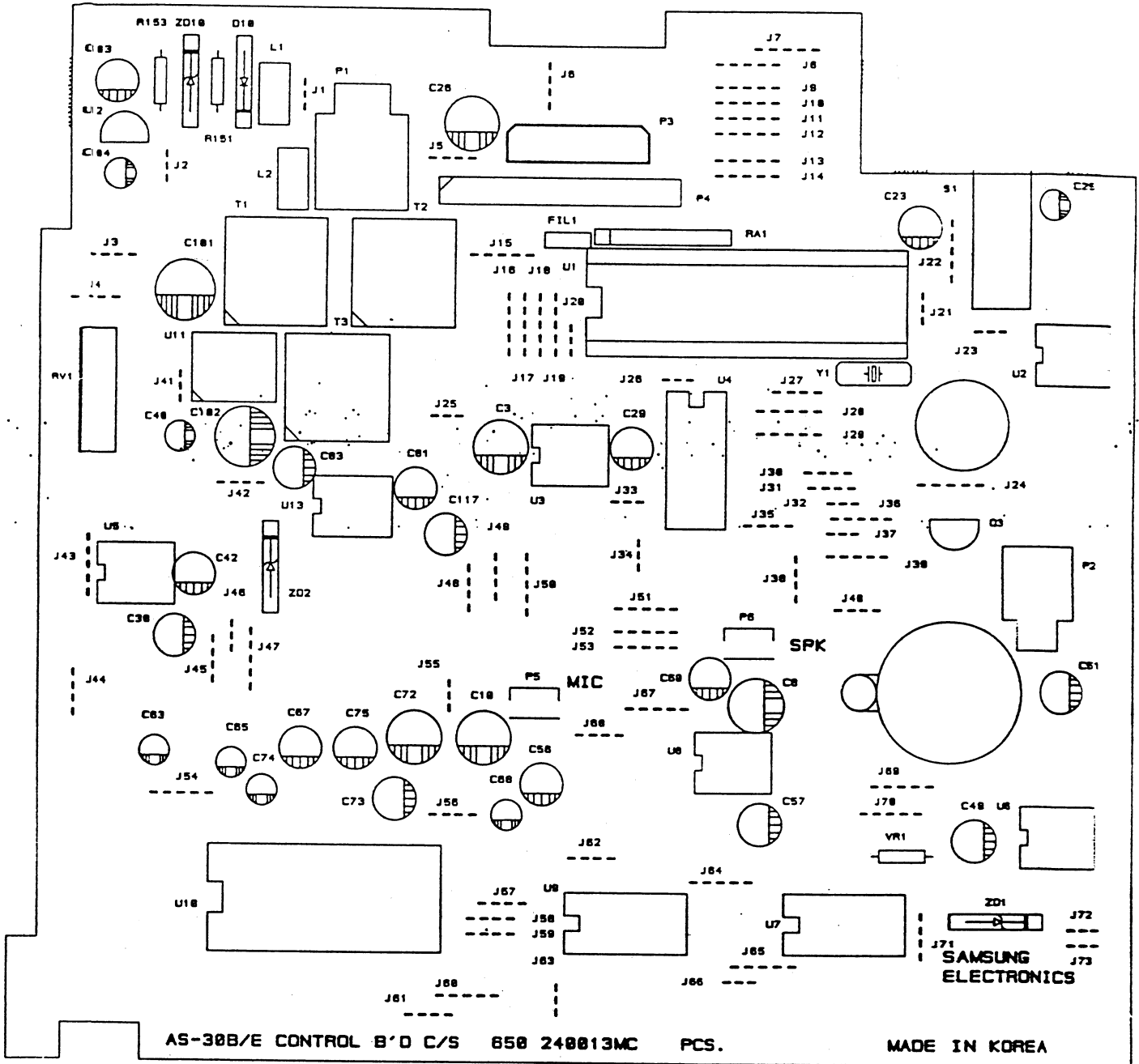
AS-11/30BV, EV Control Board C/S Component Layout



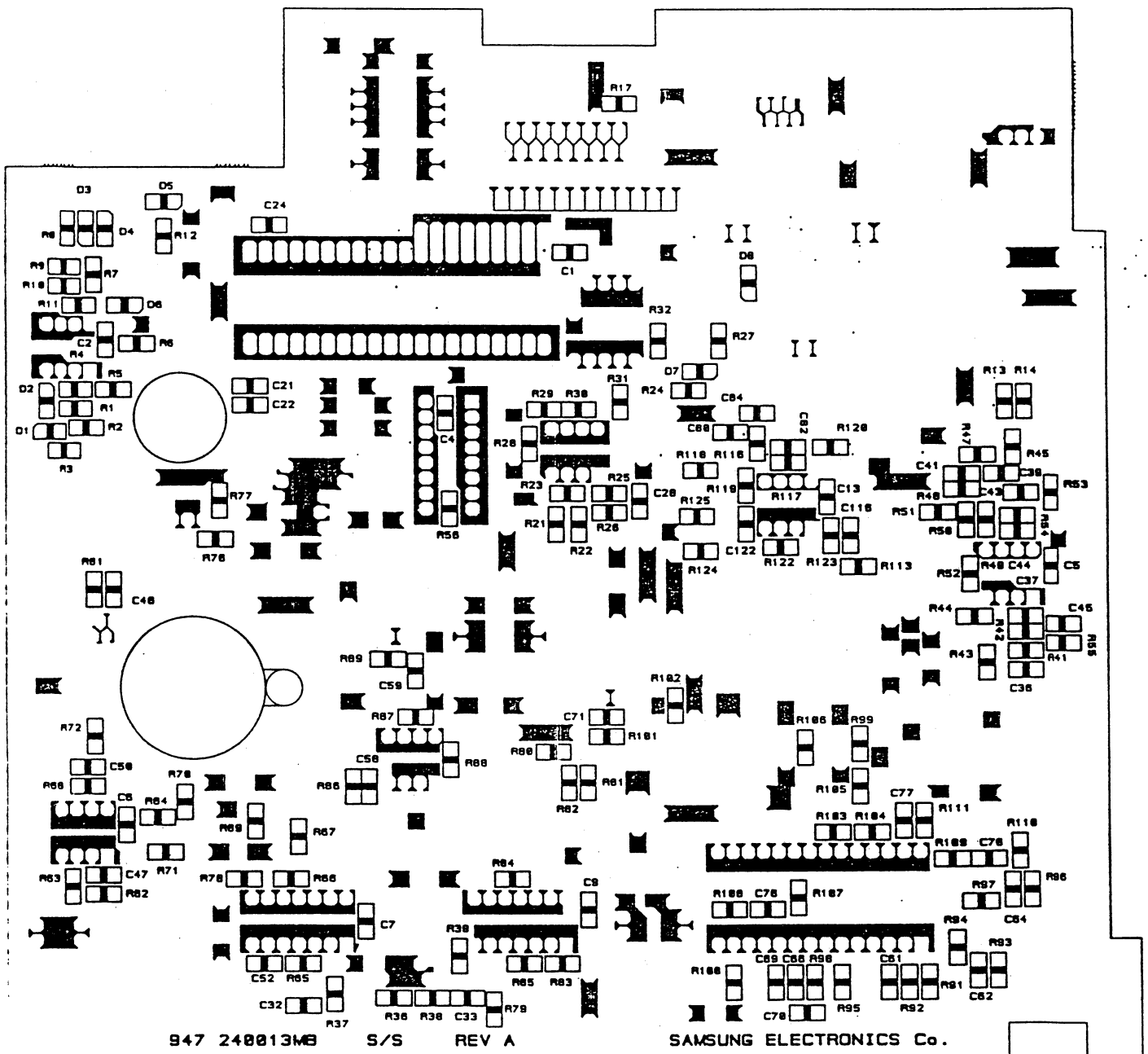
AS-11/30BV, EV Control Board S/S Component Layout



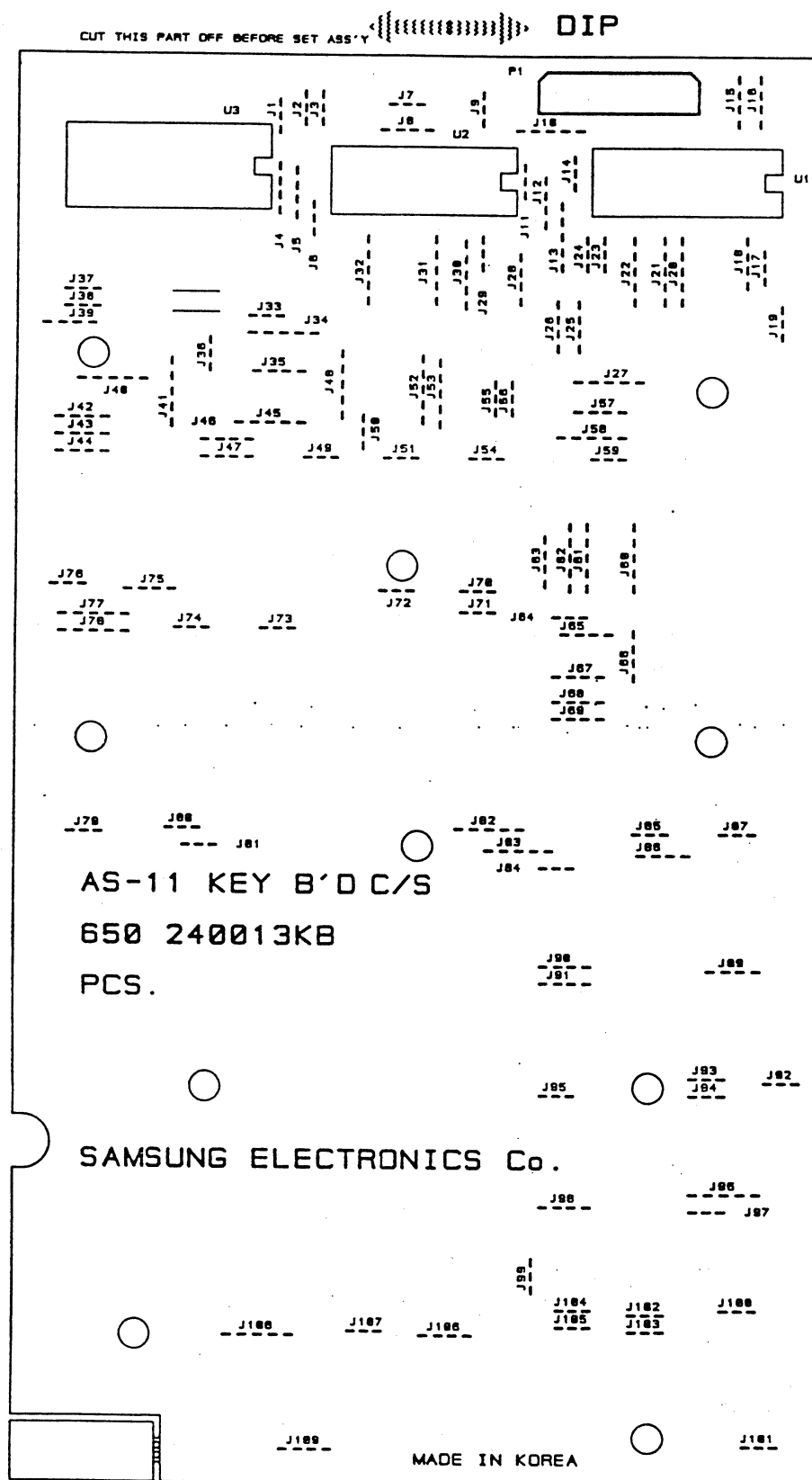
AS-11/30B, E Control Board C/S Component Layout



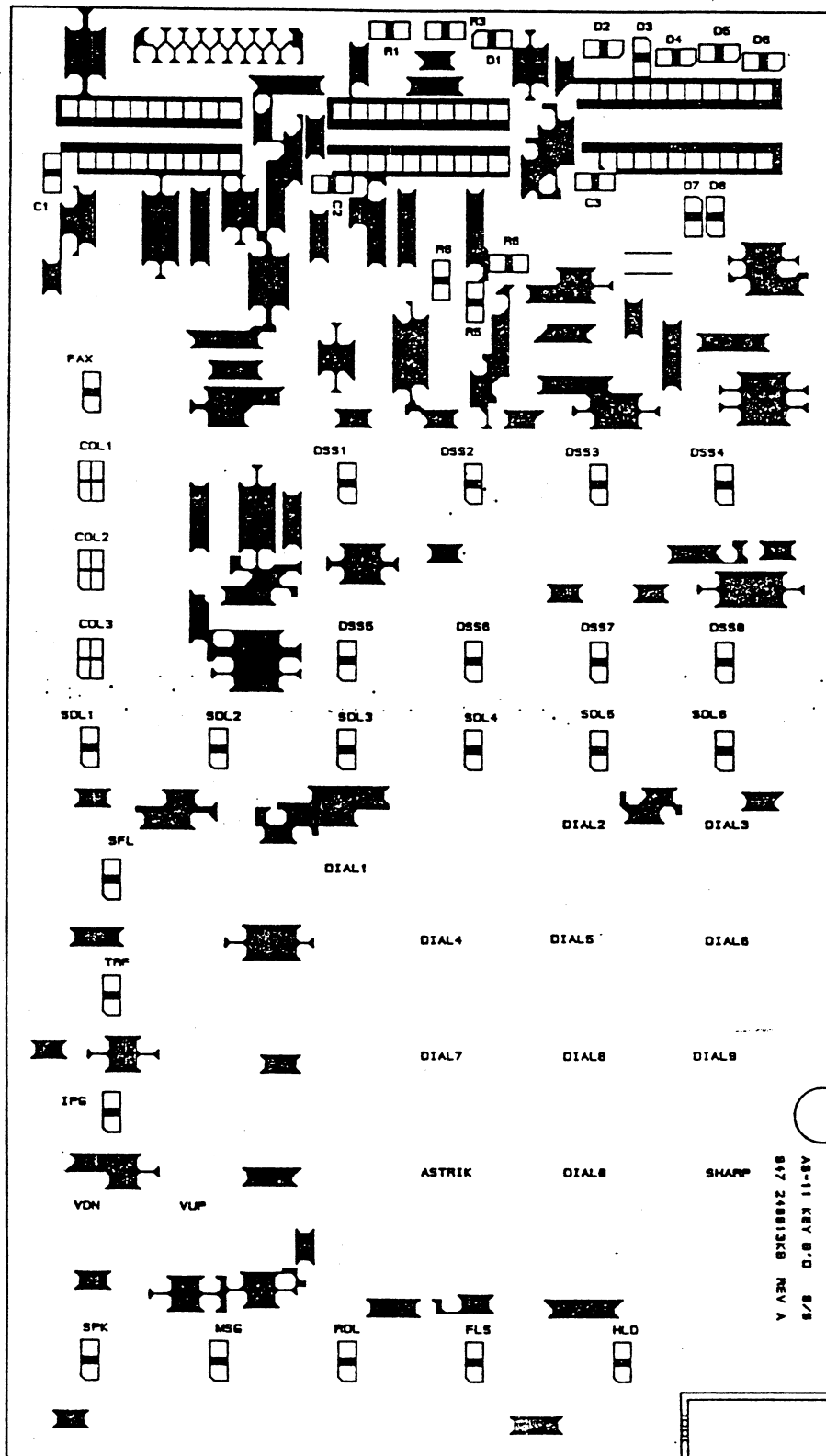
AS-11/30B, E Control Board S/S Component Layout



AS-11B, E, BV, EV Key Board C/S Component Layout



AS-11B, E, BV, EV Key Board S/S Component Layout



5. ELECTRICAL PARTLIST

NOTE : Passive devices are not described.

FFR - Forecasting Failure Rate per system.

A. PARTLIST OF KSU BOARDS

SEC CODE	DESCRIPTION	PART LOCATION	REPLACEABLE PART	FFR
873 205801AA	5801, DRIVER	U17B, U18B	SPR/UCN5801A	.005
873 790004AA	74HCT04, INVERT	U27B, U28B, U29B	HAR/CD74HCT04E PHI/PC74HCT04P	.001
873 790008AA	74HCT08, GATE	U30B	HAR/CD74HCT08E PHI/PC74HCT08P	.001
873 790138AA	74HCT138, DECODE	U11B	HAR/CD74HCT138E PHI/PC74HCT138P	.002
873 790154AB	74HCT154, DECODE	U10B	HAR/CD74HCT154EN PHI/PC74HCT154P3	.002
873 790244AA	74HCT244, BUFFER	U13B, U15B, U16B	HAR/CD74HCT244E PHI/PC74HCT244P	.005
873 790245AA	74HCT245, TRANS	U5B	HAR/CD74HCT245E PHI/PC74HCT245P	.001
873 790373AA	74HCT373, LATCH	U2B	HAR/CD74HCT373E PHI/PC74HCT373P	.001
873 790374AA	74HCT374, F/F	U8B, U12B, U19B, U20B	HAR/CD74HCT374E PHI/PC74HCT374P	.002
877 108031AA	8031, CPU	U1B	INTEL/P8031AH SIG/SCN8031AH40	.001
877 906242AA	6242, RTC	U6B	OKI/MSM6242RS	.001
881 103403AA	3403, OP AMP	U31B, U33B, U53B	MOT/MC3403P SEC/MC3403N	.001

NOTE : SUFFIX -B[BASE B'D], -P[POWER B'D]

SEC CODE	DESCRIPTION	PART LOCATION	REPLACEABLE PART	FFR
881 200393AA	393, COMPARATOR	U4P, U9P	NSC/LM393N SEC/LM393N	.001
881 201232AA	1232, MOMITOR	U48B	CD1232	
881 307812KA	7812, REGULATOR	U5P	MOT/MC7812CT SEC/MC7812CT	.001
881 307824KA	7824, REGULATOR	U52B, U8P	MOT/MC7824CT SEC/MC7824CT	.001
881 307840AA	78S40, REGULATOR	U10P	MOT/UA78S40PC SEC/KA78S40N	.001
881 307905KA	7905, REGULATOR	U7P	MOT/MC7905CT SEC/MC7905CT	.001
881 522100AA	22100, NETWORK	U9B	HAR/CD22100BE MOT/MC142100CP	.003
881 602413AB	2413, GENERATOR	U54B	SEC/KA2413B	.001
881 603494AA	3494, NETWORK	U7B	SGS/M3494B2	.005
881 605900AA	5900, DECODER	U22B	SIG/NE5900N	.001
881 608870AA	8870, RECEIVER	U23B, U34B, U25B	MITEL/MT8870CE SEC/KT3170N	.001
881 700993AA	993, DEFLECTION	U26B	RMC/RTS993-8	.001
881 900556AA	NE556, TIMER	U1P	NE556	
883 162256AA	62256, SRAM	U4B	MOT/MCM60256AP12	.001
883 627512BA	27512, EPROM	U3B	AMD/AM27512DC255 INTEL/D27512	.001
887 115273SF	R-NETWORK, 8P	RA4B	BECK/M8-3-273J DANAM/DA08S273IJ	.001
887 115683SF	R-NETWORK, 8P	RA3B	BECK/M8-3-683J DANAM/DA08S683IJ	.001
887 135103SG	R-NETWORK, 9P	RA1B, RA2B, RA8B 1UB	BECK/M9-1-103J DANAM/DA09S103CJ	.001

NOTE : SUFFIX -B[BASE B'D], -P[POWER B'D]

SEC CODE	DESCRIPTION	PART LOCATION	REPLACEABLE PART	FFR
.87 190016SH	R-NETWORK,10P	RA5B, RA6B	DANAM/10S301F2W	.001
887 400039SA	HYB,DC BY-PASS	U45B - U47B	DANAM/KP-0039SA Y.Y/KP-0039SA	.002
887 400074SA	HYB,DATA TX/RX	U34B - U35B	DANAM/HYB-1	.002
887 400212AA	HYB,SLC INTERF	U38B - U44B	TYC/SLC-01	.002
887 408301AA	HYB,REGULATOR	U6P	SANKE/SI8301L	.001
891 190002AA	TR-PNP,KSA709	Q7B, Q8P, Q10P	SEC/KSA709-Y	.002
891 290006AB	TIP42C,2W	Q2P, Q15P	MOT/TIP42C SEC/TIP42C	.001
891 390003AB	TR-NPN,KSC1009	Q8B, Q9P, Q11P, Q12P	SEC/KSC1009-Y	.002
891 490009AA	TIP41C,2W	Q13P	MOT/TIP41C SEC/TIP41C	.001
891 550675AA	2SB675Z	Q1P		.001
893 114148AA	DIODE-SIG,4148	D1B - D10B, D100B D2P - D5P	DSMS/1N4148 PHI/1N4148	.001
93 210749AB	DIODE-ZEN,749A	ZD1B - ZD22B, ZD36B - ZD39B	MOT/1N749A	.001
893 214370AB	DIODE-ZEN,4370A	ZD2P	ITT/1N4370A MOT/1N4370A	.001
893 214370AB	1N4730	ZD29B - ZD33B	ITT/1N4730A MOT/1N4730A	.001
893 214735AB	DIODE-ZEN,4735A	ZD1P	ITT/1N4735A MOT/1N4735A	.001
893 214749AB	1N4749A	ZD3P	ITT/1N4749A MOT/1N4749A	.001

NOTE : SUFFIX -B[BASE B'D], -P[POWER B'D]

SEC CODE	DESCRIPTION	PART LOCATION	REPLACEABLE PART	FFR
893 214751AB	DIODE-ZEN,4751A	ZD23B - ZD28B	ITT/1N4751A MOT/1N4751A	.001
893 314004AA	DIODE-REC,4004	D6P - D8P, D19B	DSMS/DS4004 MOT/1N4004	.001
893 315401AA	DIODE-REC,5401	D1P, D9P	GI/1N5401 MOT/1N5401	.001
893 315822AA	DIODE-REC,5822	D10P	GI/1N5822 MOT/1N5822	.001
893 390108AA	DIODE-REC,W02M	BD2P,BD4P	FAGOR/W02F GI/W02M	.001
893 390138AA	DIODE-REC,RS403	BD1P	RECT/RS403L	.001
895 110002RA	LED,ROUND	LED1B	ROHMK/SLR 54URC KEC/KLR114E	.001
895 520827AA	OPT-COUP.PC827	U2P, U3P	SHARP/PC827 KEC/PC827	.003
895 530002AA	OPT-COUP,PC817	U49B - U51B	SHARP/PC817 KEC/PC817 TSB/TLP621	.003
897 110502AB	THER,6.8,19.5MM	PSW2P	MUR/PTH63AR6R8M2 B491	.001
897 110506AA	THER,0.259,DISK	PSW3P	RAY/RDE070A	.001
897 110506XB	THERMISTOR	PSW1P, PSW1B - PSW9B	RAY/21117	.001
897 130500AA	VARI,390V	VAR25B - VAR33B	HAR/V250LA4 MAT/ERZ-C07DK391	.001
897 130507AK	VARI,470V	VAR2P, VAR3P	MAT/ERZ-C07DK471	.001

NOTE : SUFFIX -B[BASE B'D], -P[POWER B'D]

SEC CODE	DESCRIPTION	PART LOCATION	REPLACEABLE PART	FFR
913 451007FA	R-VAR,10K	VR1B	BECK/82MR10K COSMO/GFP061B10K	.001
923 110017AB	TRF-AF,600//600	T9B - T16B, T1P	SJET/5692	.002
923 110548AB	TRF 2400//600	T2P	SJET/ST-1AB	.002
923 110028AC	TRF-AF,2400//60	T1B - T8B, T17B - T19B	SJET/ST-1C	.003
925 210042AA	IND-AF,300UH	L1P, L2B	DHELO/LF-1 SWE/LF-1	.001
927 300503ABNA	RELAY,24V,2FORM	K2B - K8B, K13B	TAKAM/RV24W-K	.001
927 300513AC	RELAY,24V,2FORM	K17B, K18B	TAKAM/RV24W-K	.001
927 300513DCNA	RELAY,24V,1FORM	K9B - K11B	MAT/DS1E-M-DC24V	.001
935 200550AB	CON-MICRO,50P	P4B	AMP/552726-1	.001
935 220103CE	CON-HEADER,3P	J2B - J8B, J10B - J16B J18B - J24B, J26B - J39B	MOLEX/2258-1503 WY/SPS04-S03B	.001
935 720019BASA	MODULAR JACK	P1B - P3B	6P4C	
935 720053AA	PHONE JACK	P5		
937 120102AB	MAG-BEAD		SAMH	.001
941 110040AA	CRYSTAL,11.059M	Y1B	ITC/HC49U,11.059 SUN/HC18U,11.059	.002
941 110504AA	CRYSTAL,32.768K	Y2B	DAIWA/DT-38 SEIK/C-002RX	.002
941 110511AA	CRYSTAL,3.5795M	Y3B - Y4B	ITC/HC49U,3.5795 SUN/HC18U,3.5795	.002
953 130018AA	BAT-NICD,60MA	BT1B	VAR/53306-303024	.001

NOTE : SUFFIX -B[BASE B'D], -P[POWER B'D]

B. PARTLIST OF KSU MISCELLANEOUS

SEC CODE	DESCRIPTION	REPLACEABLE PART	FFR
135 006014AAAA	INSTALLATION & PROGRAMMING MANUAL WITH INFOR	135 006014AAAA	
923 130034AB	TRF, POWER, 110/220//DC8V/24V	923 130034AB	.001
933 130020DA	SWITCH-ROCKER, DPST, 250V	933 130020DA	.001
935 710507AA	CON-PLUG, U-RINK, 2LINE	935 710507AA	.001
949 110512AB	FUSE-GLASS TUBE, 1A, 250V, SLOW-BLOW	LIT/313 001 SHF/61T-250V1A	.001
953 260018BA	FUSE HOLDER, 10A, 250V	SHF/FH-61AS	.001
955 350320AA	CBF, PWR CORD ASS'Y	955 350320AA	.001

C. PARTLIST OF KEYSSET BOARDS

SEC CODE	DESCRIPTION	PART LOCATION	REPLACEABLE PART	FFR
873 205801AA	5801, DRIVER	U3K	SPR/UCN5801A	.002
873 404066AA	4066, SWITCH	U7M, U9M	GSS/GD4066B MOT/MC14066BCP	.001
873 790373AA	74HCT373, LATCH	U1K, U2K, U14V	HAR/CD74HCT373E PHI/PC74HCT373P	.001
877 808051AM	CPU, 8051, AS-30	U1M	877 808051AM	.001
881 105532AA	5532, DUAL OPAMP	U3M, U5M, U6M, U13M	RAY/RC5532NB SEC/KA5532CN	.001
881 200393AA	393, COMPARATOR	U2M	NSC/LM393N SEC/LM393N	.001
881 307812TA	7812, REGULATOR	U12M	MOT/MC78L12ACP SEC/MC78L12ACZ	.001
881 522100AA	22100, SWITCH	U4M	HAR/CD22100BE MOT/MC142100CP	.001
881 634018AA	34018, SPK-PHONE	U10M	MOT/MC34018P	.001
881 700386AA	386, SPK DRIVER	U8M	NSC/LM386N-1 SEC/LM386N	.001
881 705917EA	5917, VMS	U15V	SEC/KS5917	.002
883 241256AB	41256, DRAM	U16V - U19V	HIT/HM50256P-15 SEC/KM41256AP-15	.001
887 135473SG	R-NETWORK, 47K	RA1M	BECK/M9-1-473J DANAM/DA09S473CJ	.001
887 408201AA	HYB, REGULATOR	U11M	SANKEN/SI8201L	.001
891 390003AB	TR-NPN, KSC1009Y	Q3M, Q5M	SEC/KSC1009-Y	.001
893 194148AB	DIODE-SIG, 120TR	D1K - D8K, D1M - D8M	HIT/HSK120TR ROHM/RLS4148	.001
893 214732AB	DIODE-ZEN, 4732A	ZD1M, ZD2M	ITT/1N4732A MOT/1N4732A	.001
893 214752AB	DIODE-ZEN, 4752A	ZD10M	ITT/1N4752A MOT/1N4752A	.001
893 314004AA	DIODE-REC, 4004	D10M	DSMS/DS4004 MOT/1N4004	.001

NOTE : SUFFIX -M[CONTROL B'D] -K[KEY B'D] -V[CONTROL B'D WITH VMS]

SEC CODE	DESCRIPTION	PART LOCATION	REPLACEABLE PART	FFR
895 190004DA	LED,DUAL,R/Y	COL1K - COL12K	STAN/BRPY1201W-1	.00.
895 190005RA	LED,SINGLE,RED	SDL1K - SDL18K, FLSK, HLDK, IPGK, RDLK, SFLK, SPKK, TRFK MSGK	STAN/BR1102W	.003
897 130505AB	VARI,1.5V,0.3W	VR1M	DSMS/VR60	.001
923 110017AB	TRF-AF,600//600	T1M - T3M	SJET/5692	.001
933 210065AA	SW-HOOK,SPST	S1M	HOSID/HXW3951-01	.001
935 144114AANA	CON-FLAT,14P	P4M	BURN/HLEM 14S-1	.001
935 144117FD	CON-FLAT,17P	P1K, P3M	ELCOK/8370-171	.001
935 240102AA	CON-HEAD,2P	P5M, P6M	DUPON/67094-002	.00
935 720021BASA	CON-JACK,6P/6C	P1M	DEE/623PCB6-C(S)	.001
935 720021CASA	CON-JACK,4P/4C	P2M	DEE/616PCB4-C(S)	.001
941 110040AA	CRYSTAL,11.059M	Y1M	ITC/HC49U,11.059 SUN/HC18U,11.059	.001
943 150021TL	FILTER-LPF,103	FIL1M	SAMH/CFI06B103MF	.001

NOTE : SUFFIX -M[CONTROL B'D] -K[KEY B'D] -V[CONTROL B'D WITH VMS]

D. PARTLIST OF KEYSET MISCELLANEOUS

SEC CODE	DESCRIPTION	REPLACEABLE PART	FFR
135 006014BAAA	USER'S GUIDE FOR AS-11	135 006014BAAA	
137 201203HLCD	LCD ASS'Y,1 LINE 16 CHARACTER WITH CONNECTOR	137 201203HLCD	.001
137 201299BAAA	HANDSET ASS'Y, ALMOND COLOR	137 201299BAAA	.001
821 240105BA	PLT,GUIDE COVER	821 240105BA	.001
829 240004BB	MMP,GUIDE PAPER,SNOW WHITE	829 240004BB	.001
935 910008FA	CON,CONNECTING BLOCK,6P	935 910008FA	.001
955 250462PENW	CBF,HANDSET CORD,ALMOND,300MM	955 250462PENW	.001
955 250481RAEG	CBF,LINE CORD,ALMOND,4P,4300MM	955 250481RAEG	.001
955 250482PBAA	CBF,HANDSET CORD,ALMOND,4P,450MM	955 250482PBAA	.001
955 250643SAEG	CBF,LINE CORD,ALMOND,6P,4300MM	955 250643SAEG	.001
955 251460FAJZ	CBF,FLEXIBLE,14P,2.54 PITCH,LCD CABLE	FUJI/TWVF14-80 HIT/CUJ(2896)14F	.001
955 251774FAFZ	CBF,FLEXIBLE,17P,1.25 PITCH,KEY CABLE	FUJI/TWVF17-50 HIT/HCUJ(1.25)17	.001

6 . COMPONENT PIN ASSIGNMENT

CONTENTS

8031/8051	174
27512	
M3494B2	175
KM62256	
74HCT154	176
UCN5801A	
LM393	
74HCT373	177
74HCT374	
74HCT244 .	
74HCT04	
74HCT138	178
74HCT08	
NE5900	
MSM6242RS	179
KA2413B	
MT8870CE	
CD22100	180
74HCT245	
MC3403	181
MC34018	
LM386	
4066	182
KS5917	

8 0 3 1 or 8 0 5 1**8-bit Micro-controller, 40 DIP**

P1.0	<==>	□	1	40	□	<==>	VCC
P1.1	<==>	□	2	39	□	<==>	P0.0/AD0
P1.2	<==>	□	3	38	□	<==>	P0.1/AD1
P1.3	<==>	□	4	37	□	<==>	P0.2/AD2
P1.4	<==>	□	5	36	□	<==>	P0.3/AD3
P1.5	<==>	□	6	35	□	<==>	P0.4/AD4
P1.6	<==>	□	7	34	□	<==>	P0.5/AD5
P1.7	<==>	□	8	33	□	<==>	P0.6/AD6
RESET	==>	□	9	32	□	<==>	P0.7/AD7
P3.0/RXD	<==>	□	10	31	□	<==	EA/VP
P3.1/TXD	<==>	□	11	30	□	<==>	ALE/P
P3.2	<==>	□	12	29	□	==>	PSEN
P3.3	<==>	□	13	28	□	<==>	P2.7/A15
P3.4	<==>	□	14	27	□	<==>	P2.6/A14
P3.5	<==>	□	15	26	□	<==>	P2.5/A13
P3.6/WR	<==>	□	16	25	□	<==>	P2.4/A12
P3.7/RD	<==>	□	17	24	□	<==>	P2.3/A11
XTAL2	<==	□	18	23	□	<==>	P2.2/A10
XTAL1	==>	□	19	22	□	<==>	P2.1/A9
GND	<==>	□	20	21	□	<==>	P2.0/A8

2 7 5 1 2**64 Kbyte EPROM, 28 DIP**

A15	==>	□	1	28	□	<==>	VCC
A12	==>	□	2	27	□	<==	A14
A7	==>	□	3	26	□	<==	A13
A6	==>	□	4	25	□	<==	A8
A5	==>	□	5	24	□	<==	A9
A4	==>	□	6	23	□	<==	A11
A3	==>	□	7	22	□	<==	OE
A2	==>	□	8	21	□	<==	A10
A1	==>	□	9	20	□	<==	CS
A0	==>	□	10	19	□	==>	D7
D0	<==	□	11	18	□	==>	D6
D1	<==	□	12	17	□	==>	D5
D2	<==	□	13	16	□	==>	D4
GND	<==>	□	14	15	□	==>	D3

M 3 4 9 4 B 2

8 by 16 Cross-points, 40 DIP

Y3	<==>	☐	1	40	☐	<==>	VDD
AY2	==>	☐	2	39	☐	<==>	Y2
RST	==>	☐	3	38	☐	<==	DATA
AX3	==>	☐	4	37	☐	<==>	Y1
AX0	==>	☐	5	36	☐	<==	C/S
X14	<==>	☐	6	35	☐	<==>	Y0
X15	<==>	☐	7	34	☐		N.C
X6	<==>	☐	8	33	☐	<==>	X0
X7	<==>	☐	9	32	☐	<==>	X1
X8	<==>	☐	10	31	☐	<==>	X2
X9	<==>	☐	11	30	☐	<==>	X3
X10	<==>	☐	12	29	☐	<==>	X4
X11	<==>	☐	13	28	☐	<==>	X5
N.C		☐	14	27	☐	<==>	X12
Y7	<==>	☐	15	26	☐	<==>	X13
GND	<==>	☐	16	25	☐	<==	AY1
Y6	<==>	☐	17	24	☐	<==	AY0
CS	==>	☐	18	23	☐	<==	AX2
Y5	<==>	☐	19	22	☐	<==	AX1
VBB	<==>	☐	20	21	☐	<==>	Y4

K M 6 2 2 5 6

32 Kbyte SRAM, 28 DIP

A14	==>	☐	1	28	☐	<==>	VCC
A12	==>	☐	2	27	☐	<==	WE
A7	==>	☐	3	26	☐	<==	A13
A6	==>	☐	4	25	☐	<==	A8
A5	==>	☐	5	24	☐	<==	A9
A4	==>	☐	6	23	☐	<==	A11
A3	==>	☐	7	22	☐	<==	OE
A2	==>	☐	8	21	☐	<==	A10
A1	==>	☐	9	20	☐	<==	CS
N.C		☐	10	19	☐	==>	D7
D0	<==	☐	11	18	☐	==>	D6
D1	<==	☐	12	17	☐	==>	D5
D2	<==	☐	13	16	☐	==>	D4
GND	<==>	☐	14	15	☐	==>	D3

7 4 H C T 1 5 4

4 to 16 Decoder, 24 DIP

Y0	<==	□	1	24	□	<==>	VCC
Y1	<==	□	2	23	□	<==	A
Y2	<==	□	3	22	□	<==	B
Y3	<==	□	4	21	□	<==	C
Y4	<==	□	5	20	□	<==	D
Y5	<==	□	6	19	□	<==	G2
Y6	<==	□	7	18	□	<==	G1
Y7	<==	□	8	17	□	==>	Y15
Y8	<==	□	9	16	□	==>	Y14
Y9	<==	□	10	15	□	==>	Y13
Y10	<==	□	11	14	□	==>	Y12
GND	<==>	□	12	13	□	==>	Y11

U C N 5 8 0 1 A

8 Darlington TR Array, 22 DIP

CLR	==>	□	1	22	□	<==	OE
LE	==>	□	2	21	□	<==>	VDD
D0	==>	□	3	20	□	==>	Q1
D1	==>	□	4	19	□	==>	Q1
D2	==>	□	5	18	□	==>	Q2
D3	==>	□	6	17	□	==>	Q3
D4	==>	□	7	16	□	==>	Q4
D5	==>	□	8	15	□	==>	Q5
D6	==>	□	9	14	□	==>	Q6
D7	==>	□	10	13	□	==>	Q7
GND	<==>	□	11	12	□	<==	DI

L M 3 9 3Dual Comparator
8 DIP

OUT1	<==	□	1	8	□	<==>	VCC
(-)1	==>	□	2	7	□	==>	OUT2
(+)1	==>	□	3	6	□	<==	(-)2
VBB	<==>	□	4	5	□	<==	(+)2

7 4 H C T 3 7 3
7 4 H C T 3 7 4

Octal Latch, state, 20 DIP
Octal Latch, edge, 20 DIP

OE	==>	☐	1	20	☐	<==>	VDD
Q0	<==	☐	2	19	☐	==>	Q7
D0	==>	☐	3	18	☐	<==	D7
D1	==>	☐	4	17	☐	<==	D6
Q1	<==	☐	5	16	☐	==>	Q6
Q2	<==	☐	6	15	☐	==>	Q5
D2	==>	☐	7	14	☐	<==	D5
D3	==>	☐	8	13	☐	<==	D4
Q3	<==	☐	9	12	☐	==>	Q4
GND	<==>	☐	10	11	☐	<==	CLK

7 4 H C T 2 4 4

Octal Buffer, 20 DIP

1G	==>	☐	1	20	☐	<==>	VDD
1A1	==>	☐	2	19	☐	<==	2G
2Y4	<==	☐	3	18	☐	==>	1Y1
1A2	==>	☐	4	17	☐	<==	2A4
2Y3	<==	☐	5	16	☐	==>	1Y2
1A3	==>	☐	6	15	☐	<==	2A3
2Y2	<==	☐	7	14	☐	==>	1Y3
1A4	==>	☐	8	13	☐	<==	2A2
2Y1	<==	☐	9	12	☐	==>	1Y4
GND	<==>	☐	10	11	☐	<==	2A1

7 4 H C T 0 4

6 Inverter, 14 DIP

1A	==>	☐	1	14	☐	<==>	VDD
1Y	<==	☐	2	13	☐	<==	6A
2A	==>	☐	3	12	☐	==>	6Y
2Y	<==	☐	4	11	☐	<==	5A
3A	==>	☐	5	10	☐	==>	5Y
3Y	<==	☐	6	9	☐	<==	4A
GND	<==>	☐	7	8	☐	==>	4Y

7 4 H C T 1 3 8

3 to 8 Decoder, 16 DIP

A	==>	☐	1	16	☐	<==>	VDD
B	==>	☐	2	15	☐	==>	Y0
C	==>	☐	3	14	☐	==>	Y1
G2A	==>	☐	4	13	☐	==>	Y2
G2B	==>	☐	5	12	☐	==>	Y3
G1	==>	☐	6	11	☐	==>	Y4
Y7	<==	☐	7	10	☐	==>	Y5
GND	<==>	☐	8	9	☐	==>	Y6

7 4 H C T 0 8

Quad 2 Input AND Gate, 14 DIP

1A	==>	☐	1	14	☐	<==>	VDD
1B	==>	☐	2	13	☐	<==	4B
1Y	<==	☐	3	12	☐	<==	4A
2A	==>	☐	4	11	☐	==>	4Y
2B	==>	☐	5	10	☐	<==	3B
2Y	<==	☐	6	9	☐	<==	3A
GND	<==>	☐	7	8	☐	==>	3Y

N E 5 9 0 0

Tone Decoder, 16 DIP

IN	==>	☐	1	16	☐	<==>	VDD
REF	<==>	☐	2	15	☐		N.C
XTAL1	==>	☐	3	14	☐	<==	CS
XTAL2	<==	☐	4	13	☐		N.C
N.C		☐	5	12	☐	==>	D1
CLR	==>	☐	6	11	☐	==>	D2
N.C		☐	7	10	☐	==>	D3
GND	<==>	☐	8	9	☐	==>	DV

MSM6242RS

Real Time Clock, 18 DIP

STD.P	<==>	☐	1	18	☐	<==>	VDD
CS0	==>	☐	2	17	☐	==>	XTAL2
ALE	==>	☐	3	16	☐	<==	XTAL1
A0	==>	☐	4	15	☐	<==	CS1
A1	==>	☐	5	14	☐	<==>	D0
A2	==>	☐	6	13	☐	<==>	D1
A3	==>	☐	7	12	☐	<==>	D2
RD	==>	☐	8	11	☐	<==>	D3
GND	<==>	☐	9	10	☐	<==	WR

KA2413B

DTMF Sender, 16 DIP.

XTAL1	==>	☐	1	16	☐	<==	D7
XTAL2	<==	☐	2	15	☐	<==	D6
RL	<==>	☐	3	14	☐	<==	D5
RH	<==>	☐	4	13	☐	<==	D4
C1	<==>	☐	5	12	☐	<==	D3
C2	<==>	☐	6	11	☐	<==	D2
GND	<==>	☐	7	10	☐	<==	D1
OUT/VDD	<==>	☐	8	9	☐	<==	D0

MT8870CE

DTMF Receiver, 18 DIP

IN+	==>	☐	1	18	☐	<==>	VDD
IN-	==>	☐	2	17	☐	==>	ST/GT
GS	<==>	☐	3	16	☐	==>	EST
VR	<==>	☐	4	15	☐	==>	STD
INH	==>	☐	5	14	☐	==>	Q4
PWDN	==>	☐	6	13	☐	==>	Q3
XTAL1	==>	☐	7	12	☐	==>	Q2
XTAL2	<==	☐	8	11	☐	==>	Q1
GND	<==>	☐	9	10	☐	<==	TOE

CD 2 2 1 0 0**4 by 4 cross-points, 16 DIP**

X2	<==>	☐	1	16	☐	<==>	VDD
DATA	==>	☐	2	15	☐	<==>	Y1
C	==>	☐	3	14	☐	<==>	Y2
D	==>	☐	4	13	☐	<==>	X4
B	==>	☐	5	12	☐	<==>	X3
A	==>	☐	6	11	☐	<==>	Y4
CS	==>	☐	7	10	☐	<==>	Y3
GND	<==>	☐	8	9	☐	<==>	X1

7 4 H C T 2 4 5**Octal Bus Transceiver, 20 DIP**

DIR	==>	☐	1	20	☐	<==>	VDD
A0	<==>	☐	2	19	☐	<==>	OE
A1	<==>	☐	3	18	☐	<==>	B0
A2	<==>	☐	4	17	☐	<==>	B1
A3	<==>	☐	5	16	☐	<==>	B2
A4	<==>	☐	6	15	☐	<==>	B3
A5	<==>	☐	7	14	☐	<==>	B4
A6	<==>	☐	8	13	☐	<==>	B5
A7	<==>	☐	9	12	☐	<==>	B6
GND	<==>	☐	10	11	☐	<==>	B7

MC 3 4 0 3

Quad OP-AMP, 14 DIP

OUT1	<==	☐	1	14	☐	<==>	OUT4
(-)1	==>	☐	2	13	☐	==>	(-)4
(+)1	==>	☐	3	12	☐	<==	(+)4
VCC	<==>	☐	4	11	☐	<==	VBB
(+)2	==>	☐	5	10	☐	<==>	(+)3
(-)2	==>	☐	6	9	☐	<==>	(-)3
OUT2	==>	☐	7	8	☐	<==>	OUT3

MC 3 4 0 1 8

Speaker-phone Chip, 28 DIP

RR	<==>	☐	1	28	☐	<==>	RRX
RTX	<==>	☐	2	27	☐	<==	RXI
TXI	==>	☐	3	26	☐	==>	RXO
TXO	<==	☐	4	25	☐	<==>	ACF
TLI	==>	☐	5	24	☐	<==	VLC
TLO	<==>	☐	6	23	☐	<==>	XDC
RLI	==>	☐	7	22	☐	<==>	GND
RLO	<==>	☐	8	21	☐	==>	VB
MCI	==>	☐	9	20	☐	<==>	VCC
MCO	<==	☐	10	19	☐	<==	SKI
CP1	<==>	☐	11	18	☐	<==	CS
CP2	<==>	☐	12	17	☐	<==>	AGC
XDI	<==>	☐	13	16	☐	<==	V+
SKG	<==>	☐	14	15	☐	==>	SKO

LM 3 8 6

Speaker Driver, 8 DIP

GL1	<==>	☐	1	8	☐	<==>	GL2
(-)	==>	☐	2	7	☐		N.C
(+)	==>	☐	3	6	☐	<==>	VCC
GND	<==>	☐	4	5	☐	==>	OUT

4 0 6 6**Quad Analog Switch, 14 DIP**

I1	<==>	☐	1	14	☐	<==>	OUT4
O1	<==>	☐	2	13	☐	<==	C1
O3	<==>	☐	3	12	☐	<==	C2
I3	<==>	☐	4	11	☐	<==>	I2
C3	==>	☐	5	10	☐	<==>	O2
C4	==>	☐	6	9	☐	<==>	O4
OUT2	==>	☐	7	8	☐	<==>	I4

K S 5 9 1 7**Voice Recoding/Reproducing Processor, 48 FQP**

T S T
A E T E S G V
2 R U S A S T N R
R R 5 A W T T R T O D E
I O 6 S E O 2 T 1 P A F

▽ △ ▽ △ △ ▽ ▽ ▽ ▽ ▽ ▽ ◇

48 47 46 45 44 43 42 41 40 39 38 37
□ □ □ □ □ □ □ □ □ □ □ □

ACL ==> 1 ☐ ●
REC ==> 2 ☐
M1 ==> 3 ☐
M2 ==> 4 ☐
PS0 ==> 5 ☐
PS1 ==> 6 ☐
N.C 7 ☐
PS2 ==> 8 ☐
PS3 ==> 9 ☐
BS0 ==> 10 ☐
BS1 ==> 11 ☐
DI ==> 12 ☐

☐ 36 <== MCI
☐ 35 ==> C1
☐ 34 <== C2
☐ 33 ==> MCO
☐ 32 <==> GNDD
☐ 31 ==> DAO
☐ 30 <== ADI
☐ 29 <==> VDD
☐ 28 ==> A0
☐ 27 ==> A1
☐ 26 ==> A2
☐ 25 ==> A3

□ □ □ □ □ □ □ □ □ □ □ □
13 14 15 16 17 18 19 20 21 22 23 24

▽ ▽ ▽ ▽ ▽ ▽ ▽ ▽ ▽ ▽ ▽ ▽

E C C C C C D A A A A A
O A A A A L O 8 7 6 5 4
S S S S S K
1 2 3 4

V I I .

TROUBLE
SHOOTING

1 . D I A G N O S T I C S

The system has so many features and there are so many methods to test a feature. To describe all the features and the methods may require too many papers to include and it may be some long and boring. Therefore, the representative features related to circuitry will be explained. And, all the methods can be practised without any tool and equipment.

TO CHECK MAIN POWER

- ◆ Check the power of keyset.

If out-of-order, any visual and audible indication of all the keyset will not served.

TO CHECK 5V POWER ON BASE B'D

- ◆ Check the LED on the base board.

If out-of-order, the LED is OFF.

TO CHECK 24V POWER ON BASE B'D

- ◆ Listen to the sound of the relay during AC power ON/OFF.

During AC power ON/OFF, the sound of PFT relays may be heard. Otherwise, 24V power supply on the base board is out of order.

TO CHECK KEYSET INSTALLATION

- ◆ Check the visual or audible service at the keyset during system operation.

Any button and handset will not work if out-of-order.

- ◆ Repeat the check to all of the keysets.

TO CHECK KEYSET OPERATION

- ◆ Connect a keyset to the system.
- ◆ Run the self diagnostics described in the installation/programming manual. (Program 81)

System control part operation, Data communication, LCD display, Ring-tone generator and its gain control of keyset, Speaker gain control, and Key & LED operation can be checked.

- ◆ Repeat the check to all of the keysets.

TO CHECK MEMORY BACKUP

- ◆ Confirm that the shunt pin SP31 on the base board is selected to ON.
- ◆ Change any content of user-program. Refer to the Installation and Programming Manual.
- ◆ Check the stored content of user program after the system power OFF/ON in absence of system backup battery.

The content may be destroyed, if out-of-order.

TO CHECK SYSTEM BACKUP

- ◆ Confirm that the external rechargeable battery of which capacity is adequate is connected to the system and charged sufficiently.
- ◆ Check that the system operates well although AC power is dis-connected.

The system may not operate if the charge/recharge circuitry for the external battery is out of order.

TO CHECK REAL TIME CLOCK

- ◆ Adjust the current date/time by user programming during system operation. (Program code 55)
- ◆ Check that the time increases in one minute at the display of the keyset.

TO CHECK REAL TIME CLOCK BACKUP

- ◆ Adjust the current date/time by user programming during system operation. (Program code 55)
- ◆ Check that the date/time data is destroyed after toggling power.

TO CHECK SLT INSTALLATION

- ◆ Listen to dial tone through handset of single line telephone during system operation. Or,
- ◆ Check the related BLF at the keyset works or not during hook ON/OFF.
- ◆ Repeat the check to all the single line telephones.

TO CHECK SLT DIAL PULSE DETECTION

- ◆ Dial the adequate station number at the dial pulse single line telephone, and check the call operation. Or,
- ◆ Connect the dial pulse trunk line to single line telephone port. (Program code 42)

Approach to the trunk line, dial the adequate station number, and check the call operation.
- ◆ Repeat the check to all the single line telephones.

TO CHECK SLT DTMF DETECTION

- ◆ Dial the adequate station number at the DTMF single line telephone, and check the call operation. Or,
- ◆ Connect the DTMF trunk line to single line telephone port. (Proram code 42)
Approach to the trunk line, dial the adequate station number, and check the call operation.
- ◆ Repeat the check to all the single line telephones.

TO CHECK RING GENERATOR

- ◆ Dial the SLT station number and check the bell at the SLT. Or,
- ◆ Connect the trunk line to single line telephone port.
Dial the SLT station number and check the trunk incoming call.
(Program code 40, 60, 61, 62)

TO CHECK TONE GENERATOR

- ◆ Listen to dial tone through handset/speaker at the keyset.

TO CHECK SLT DIAL TONE SUPPLY

- ◆ Listen to dial tone through handset at three single line telephones at the same time in basic KSU.

TO CHECK TRUNK RING DETECTION

- ◆ Connect the trunk line to single line telephone port.
- ◆ Dial the SLT station number and check the trunk incoming call.
(Program code 40, 60, 61, 62)
- ◆ Repeat the check to all the loop-start trunk lines.

TO CHECK TRUNK DIAL PULSE SENDING

- ◆ Adjust the trunk dial type to Dial Pulse. (Program code 42)
- ◆ Approach to the trunk line, dial any digit, and listen to the sound of relay operation. Or,

Connect the trunk line to the single line telephone, Approach to the trunk line, Dial the adequate station number, and check the call operation.

- ◆ Repeat the check to all the trunk lines.

TO CHECK TRUNK DTMF SENDING

- ◆ Adjust the trunk dial type to DTMF. (Program code 42)
- ◆ Connect the trunk line to the single line telephone port.
- ◆ Approach to the trunk line and dial the adequate station number.
- ◆ Check the call operation.
- ◆ Repeat the check to all the trunk lines.

TO CHECK POWER FAILURE TRANSFER

- ◆ Connect the practical telephone lines to the first trunk and the second.
- ◆ Connect the single line telephones to the 7th station and 8th station.
- ◆ Dis-connect AC power and the external battery when installed.
- ◆ Check the single line telephone operations.

TO CHECK NETWORK

- ◆ Install a keyset or single line telephone to the system.
- ◆ Hook off the handset and listen to the dial tone.
- ◆ Repeat the check 13 times.

TO CHECK AUTO REDIAL

- ◆ Install some stations to the system.
- ◆ Connect a trunk line to the single line telephone port.
- ◆ Hook off the handset of station B. (Busy state)
- ◆ Approach the trunk line and dial station B number at a keyset.
- ◆ Press RD button and hang on.
- ◆ Check the call operation.

TO CHECK DOOR-PHONE OPERATION

- ◆ Install door-phone to the system.
- ◆ Adjust door-phone ring table. (Program code 63)
- ◆ Press the call button of door-phone.
- ◆ Receive the call at the ringing station.
- ◆ Check the speech path.

TO CHECK DOOR-LOCK OPERATION

- ◆ Adjust the open duration of door-lock. (Program code 58)
- ◆ Make a call to door-phone.
- ◆ Press digit 1 at the station.
- ◆ Listen to the sound of the relay operation.

TO CHECK INTERNAL MUSIC SOURCE

- ◆ Press HOLD button at the hang-on keyset.
- ◆ Listen to the music.

TO CHECK EXTERNAL MUSIC SOURCE

- ◆ Install the external music source to the system.
- ◆ Press HOLD button at the hang-on keyset.
- ◆ Listen to the music.

TO CHECK INTERNAL PAGE

- ◆ Install some keysets to the system.
- ◆ Assign the page included stations. (Program code 33)
- ◆ Press PAGE button after hook-off at the hang-on keyset.
- ◆ Announce and listen.

TO CHECK EXTERNAL PAGE

- ◆ Install external speaker with amplifier to the system.
- ◆ Press FUNC/DND button and digit 1 and 4.
- ◆ Announce and listen.

TO CHECK KEYSET HANDSET SPEECH PATH

- ◆ Hook off at the keyset.
- ◆ Press digit 2.
- ◆ Speak and listen the sidetone.

TO CHECK KEYSET SPEAKER-PHONE PATH

- ◆ Press DSS button twice at the hook-on keyset.
- ◆ Check the speaker-phone path.

TO CHECK INDIVIDUAL LOUD BELL

- ◆ Install an external speaker with amplifier to a keyset.
- ◆ Enable the individual loud bell. (Program code 36)
- ◆ Make a call to the keyset.
- ◆ Listen to the ring tone from the external speaker.

2. TROUBLE SHOOTING

So many kinds of troubles may happen in the practical site and it is very difficult to describe all the field problems in this section. But, this section includes basic troubles and their solutions. If you study all the items in this section, you may get the sufficient knowledge to shoot the difficult one. Before proceeding, prepare the circuit diagrams and some simple test equipment, multi-meter and oscilloscope.

MAIN POWER FAILURE WITH AC POWER

- ① Check the power of AC outlet.

Good : Jump to the next step.

Fail : Plug the system power cord into the other AC outlet.

- ② Check the AC Fuse.

Good : Jump to the next step.

FAIL : Replace the fuse with the same capacity and try again.

If fails again, it means that one of the DC powers is short to ground.

- ③ Check the output voltage of the connector P3(1) on the power supply board.

Good : Jump to the next step. About 35 volts.

Fail : one of the DC powers is short to ground.

- ④ Dis-connect the 4th wire of the cable and check the main power. If it operates well, And check the varistor VAR1, and the capacitors C1, C2, C3 and C4 on the power supply board and replace them.

12VDC FAILURE

- ① Check the output voltage of U5 7812 on the power board after disconnecting the output plug. (12V)

Good : Jump to the next step.

Fail : Replace U5 7812.

- ② Find the damaged component related to 12VDC and replace it. This power is mainly fed to keyset data-com circuitry and door-phone.

- 5VDC FAILURE

- ③ Check the input voltage of U7 7905 on the power board. (About -12V)

Good : Jump to the next step.
Fail : Replace U10 78S40, Q15 TIP42C, or D10 1N5822 on the power board.
- ④ Check the output voltage of U2 7905 on the connection board after disconnecting the output plug. (-5V)

Good : Jump to the next step.
Fail : Replace U7 7905.
- ⑤ Find the damaged component related to - 5VDC and replace it. This power is fed to network, speech circuitry.

5VDC FAILURE ON POWER B'D

- ③ Check the input voltage of U6 SI8301L on the power board.
(About 35 volts)

Good : Replace U6 SI8301L.
Fail : Jump to the next step.
- ④ Check the input voltage of U6 SI8301L again after disconnecting the output plug.

Good : Jump to the next step.
FAIL : Replace the capacitor C11 on the power board.
- ⑤ Check the input voltage of U6 SI8301L again after replacing the capacitor C12 on the power board.

Good : End.
Fail : Jump to the next step.
- ⑥ Find the damaged component related to 5VDC power and replace it. This job requires so much time. Approach to the logic chips first near the regulator.

24VDC FAILURE ON POWER B'D

- ③ Check the output voltage of U8 7824 on the power board after disconnecting the output plug. (24 volts)
Good : Jump to the next step.
Fail : Replace 7824.
- ④ Find the damaged component related to 24VDC power and replace it. Approach to the by-pass capacitors and UCN5801A's first.

MEMORY BACKUP FAILURE

- ① Confirm that the shunt pin J38 on the base board is selected to ON position.

Good : Jump to the next step.

Fail : Move the shunt pin to ON position.

- ② Check the shunt pin J38 contact.

Good : Jump to the next step.

Fail : Replace the shunt pin J38.

- ③ Check Rechargeable Battery.

Good : End.

Fail : Replace the rechargeable battery, BT1 on the base board.

SYSTEM BACKUP FAILURE

- ① Check the battery fuse.

Good : Jump to the next step.

Fail : Replace the battery fuse with the same capacity one.

- ② Check the voltage of external battery terminal after removing the external battery during system operation. (About 35 volts)

Good : Jump to the next step.

Fail : Repair the battery charging circuit.

- ③ Check the connection to the external battery.

Good : Jump to the next step.

Fail : Replace or repair the cable.

- ④ Check the voltage of external battery terminal with the external battery during system operation.

Good : Jump to the next step.

Fail : Wait until charging. Replace the external battery if it is not charged in a long time.

- ⑤ Repair the discharging circuit. Refer to the circuit description.

REAL TIME CLOCK FAILURE

- ① Check the RTC clock. Y2 32768Hz on the base board.
- Good : Jump to the next step.
Fail : Replace the crystal Y2 32768Hz.
- ② Check the chip select signal of RTC, U6 MSM6242BRS pin 2.
- Good : Jump to the next step.
Fail : Replace the decoder U10 74HCT154.
- ③ Replace the RTC chip U6 MSM6242BRS on the base board.

SLT DC FEEDING FAILURE

- ① Check the connections.
- Good : Jump to the next step.
Fail : Install the SLT again.
- ② Check the single line telephone.
- Good : Jump to the next step.
Fail : Replace the single line telephone.
- ③ Check all the shunt pins are selected correctly and the wires are connected correctly based on the installation instruction.
- Good : Jump to the next step.
Fail : Adjust the related shunt pins.
- ④ Check 30VDC fed to the SLT hybrid chip, SLC-01.
- Good : Replace the related hybrid chip, SLC-01.
Fail : Check 30VDC regulation circuit.

SLT DIAL PULSE DETECTION FAILURE

- ① Check the connections.
- Good : Jump to the next step.
Fail : Install the SLT again.

- ⑥ Check the single line telephone.
Good : Jump to the next step.
Fail : Replace the single line telephone.
- ⑦ Check the input terminal of the related read buffer.
Good : Jump to the next step.
Fail : Replace the related hybrid chip, SLC-01.
- ⑧ Check the chip selection signal of the read buffer.
Good : Jump to the next step.
Fail : Check the related decoder and replace it.
- ⑨ Replace the read buffer, 74HCT244.

SLT DTMF DETECTION FAILURE

- ① Check the connections.
Good : Jump to the next step.
Fail : Install the SLT again.
- ② Check the single line telephone.
Good : Jump to the next step.
Fail : Replace the single line telephone.
- ③ Can you listen the dial tone without distortion.
Good : Jump to the next step.
Fail : Check the network and the transformer. Replace the damaged part.
- ④ Check the clock of the DTMF receivers.
Good : Jump to the next.
Fail : Replace the related crystal.
- ⑤ Check the control signals of the DTMF receivers and replace the damaged component.

SLT RING SIGNAL FAILURE

- ① Check the connections.
Good : Jump to the next step.
Fail : Install the SLT again.

- ⑥ Check the single line telephone.

Good : Jump to the next step.

Fail : Replace the single line telephone.

- ⑦ Check the related relay driver, UCN5801A.

Good : Jump to the next step.

Fail : Replace the relay driver UCN5801A.

- ⑧ Check the ring signal is fed to the SLT relay.

Good : Replace the relay.

Fail : Check the ring generator.

RING GENERATOR FAILURE

- ① Check U1 NE556 pin 3 (20Hz) and pin 5 (5KHz) on the power board.

Good : Jump to the next step.

Fail : Replace U1 NE556.

- ② Check the signal thru T1 5692 and T2 ST-1AB on the power board. (5KHz)

Good : Jump to the next step.

Fail : Replace T1 or T2.

- ③ Check the transistor Q8 - Q11 on the power supply board. (20Hz)

Good : Jump to the next.

Fail : Replace them.

- ④ Check the Ring signal on output plug on the power supply board.

TONE GENERATOR FAILURE

- ① Check the network.

Good : Jump to the next step.

Fail : Replace the network chip.

- ② Check U33 MC3403 pin 8 on the base board. (360Hz)

Good : Jump to the next step.

Fail : Test the peripheral circuit and replace the damaged part.

- ③ Check U33 MC3403 pin 7 on the base board. (420Hz)

Good : Test the mixing circuit and replace the damaged part.

Fail : Repair 420Hz oscillation circuit.

SLT DIAL TONE SUPPLY FAILURE

- Ⓐ Check the impedance matching circuit, U31 on the base board.

Good : Jump to the next step.
Fail : Repair the matching circuit.

- Ⓑ Check the tone network, U9 CD22100 on the base board.

Good : Jump to the next step.
Fail : Replace the tone network.

- Ⓒ Check the speech network.

Good : Jump to the next step.
Fail : Replace the network chip.

- Ⓓ Check the protection diodes 1N749A.

Good : Jump to the next step.
Fail : Replace the zener diode, 1N749A.

- Ⓔ Check the isolating transformer.

Good : Jump to the next step.
Fail : Replace the transformer.

- Ⓕ Replace the SLT hybrid chip, SLC-01.

TRUNK RING DETECTION FAILURE

- Ⓐ Check the connections.

Good : Jump to the next step.
Fail : Install correctly.

- Ⓑ Check the varistor, 391 in the trunk interface.

Good : Jump to the next step.
Fail : Replace the arrestor and check grounding the system.

- Ⓒ Check the fusible resistors in the trunk interface.

Good : Jump to the next step.
Fail : Replace the fusible resistor.

- Ⓓ Check the diode in the trunk interface.

Good : Jump to the next step.
Fail : Replace the zener diode, 1N749A.

- ⑤ Check the ring signal path parallel to the loop relay.
Good : Jump to the next step.
Fail : Repair the path.
- ⑥ Check the input of opto-coupler, PC817.

Good : Jump to the next step.
Fail : Replace the DC-bypass hybrid chip, KP0039SA.
- ⑦ Check the output of the opto-coupler, PC817 after removing the input pattern of the read buffer, 74HCT244.

Good : Jump to the next step.
Fail : Check the by-pass capacitor and replace the capacitor or PC817.
- ⑧ Check the chip strobe of the read buffer.

Good : Replace the read buffer.
Fail : Replace the related decoder.

TRUNK ACCESS FAILURE

- ① Check the connections.

Good : Jump to the next step.
Fail : Install correctly.
- ② Check the trunk lines connected to the system. (48 or 24VDC feeding)

Good : Jump to the next step.
Fail : Connect the valid trunk line to the system.
- ③ Check user-program date on c.o. line access. (Program code 31)

Good : Jump to the next.
Fail : Adjust the user-program data.
- ④ Check the loop relay in the trunk interface.

Good : Jump to the next step.
Fail : Test the relay and its driver UCN5801A, and repair it.
- ⑤ Check DC by-pass hybrid chip KP0039SA output in the trunk interface.

Good : Test the ring detector circuit and repair it.
Fail : Replace the hybrid chip, KP0039SA.

TRUNK DIAL PULSE SENDING FAILURE

- ① Check the trunk access.
Good : Jump to the next step.
Fail : Test the trunk interface as above.
- ② Check the user-program data on dial pulse make/break rate.
(Program code 23)
Good : Jump to the next step.
Fail : Adjust make/break ratio.
- ③ Check the operation after connecting the trunk line to the SLT port.
Good : Contact to the central office.
Fail : Test CPU and its peripherals, and repair it.

TRUNK DTMF SENDING FAILURE

- ① Check the trunk access.
Good : Jump to the next step.
Fail : Test the trunk interface as above.
- ② Check the user-program data on trunk dial type. (Program code 42)
Good : Jump to the next step.
Fail : Adjust trunk dial type to DTMF.
- ③ Listen to the dial tone from the trunk line.
Good : Jump to the next step.
Fail : Test the network and the trunk speech interface, and repair it.
- ④ Check the DTMF sender driving buffer, U20 74HCT374 on the base board.
Good : Jump to the next step.
Fail : Replace the buffer.
- ⑤ Check the DTMF sender, U54 KA2413B on the base board.
Good : Jump to the next step.
Fail : Replace the DTMF sender U54 KA2413B.
- ⑥ Check the amplifiers for DTMF signals on the base board.
Good : Contact to the central office.
Fail : Repair the amplification circuit.

POWER FAILURE TRANSFER FAILURE

- ④ Check the relays K17 and K18 on the base board and replace them.

NETWORK FAULT

- ④ Check the network feeding power. (GND, 5VDC, - 5VDC)
Good : Jump to the next step.
Fail : Trace the power pattern and repair.
- ⑤ Check the chip strobe signal.
Good : Jump to the next step.
Fail : Replace the inverter, the decoder, or CPU.
- ⑥ Check the chip strobe of data latch, 74HCT374.
Good : Jump to the next step.
Fail : Replace the related decoder.
- ⑦ Check the output of the data latch 74HCT374 during network access.
Good : Replace the network chip, M3494.
Fail : Replace the data latch 74HCT374.

DOOR-PHONE FAILURE

- ④ Check the connections. (Power and speech path)
Good : Jump to the next step.
Fail : Connect correctly.
- ⑤ Confirm that the proprietary door-phone is connected.
Good : Jump to the next step.
Fail : You should install the door-phone provided by Samsung Electronics.
- ⑥ Check the user program data on door-ring table. (Program code 63)
Good : Jump to the next step.
Fail : Adjust the user program data.

④ Test the following items.

Door-phone power fault : Check the volatge between the terminals of poly-switches PSW9 on the base board, and repair the power short to GND.

Call button fault : Check the power-isolating transformer and the read buffer U15 74HCT244 on the base board.

Speech path fault : Check the power-isolating transformer, the protection zener diodes ZD38, ZD39 and the network chip on the base board.

DOOR-LOCK FAILURE

① Check the connections.

Good : Jump to the next step.

Fail : Connect correctly.

② Check the door-lock capacity.

Good : Jump to the next step.

Fail : The door-lock within the capacity specified in the installation manual can be available.

③ Check the relay K13 RY24W-K on the base board.

Good : Jump to the next step.

Fail : Replace the relay.

④ Check the relay driver U17 UCN5801A on the base board.

Good : Check the control signal of the driver

Fail : Replace the relay driver U17 UCN5801A.

INTERNAL MUSIC SOURCE FAILURE

① Check the network chip.

Good : Jump to the next step.

Fail : Replace the damaged network chip M3494.

② Check MC3403 U53 pin1 on the base board.

Good : Jump to the next step.

Fail : Check the power of MC3403 and replace it.

- ③ Check the melody chip U42 RTS993-8 and its peripherals on the base board, and replace the damaged part.

EXTERNAL MUSIC SOURCE

- ① Check the connections between the AUX jack and the external music source.
- Good : Jump to the next step.
Fail : Connect correctly.
- ② Check that the external music source provides any DC power to the output.
- Good : Jump to the next step.
Fail : Add the coupling capacitor (about 1 - 10 uF).
- ③ Check the network chip.
- Good : Jump to the next step.
Fail : Replace the damaged network chip.
- ④ Check the protection zener diodes ZD32, ZD33 on the base board.
- Good : Replace the power-isolating transformer T20 ST-1C on the base board.
Fail : Replace the zener diodes ZD32, ZD33.

INTERNAL PAGE FAILURE

- ① Check the user program data on the internal page. (Program code 32, 33, 34)
- Good : Jump to the next step.
Fail : Adjust the user program data.
- ② Check the network chips and replace the damaged part.

EXTERNAL PAGE FAILURE

- Ⓐ Check the connections.

Good : Jump to the next step.
Fail : Connect correctly.

- Ⓑ Check the external amplifier and the speaker.

Good : Jump to the next step.
Fail : Replace the external amplifier or the speaker.

- Ⓒ Check the protection zener diodes ZD36, ZD37 and the power-isolating transformer and replace the damaged part.

KEYSET POWER FAILURE

- Ⓐ Check the connections between KSU and the keyset.

Good : Jump to the next step.
Fail : Connect correctly.

- Ⓑ Check the voltage of D10 1N4004 (+) on the keyset control board. (19 - 30V)

Good : Jump to the next step.
Fail : Replace the transformers T1 - T2 5692 on the keyset control board.

- Ⓒ Check the short protection resistor R151 on the keyset control board.

Good : Jump to the next step.
Fail : Replace the resistor and try again. Find the other damaged part and replace it.

- Ⓓ Check the short protection resistor R153 on the keyset control board.

Good : Check the operation of the regulators U11 SI8201L and U12 78L12 and replace the damaged part.
Fail : Replace the resistor and try again. Find the other damaged part and replace it

KEYSET DATA-COM FAILURE

- Ⓐ Check the connections between KSU and the keyset. The data path has the polarity.

Good : Jump to the next step.

Fail : Connect correctly.

- Ⓑ Replace the keyset with the other.

Good : Jump to the next step.

Fail : Contact to the related keyset interface in the system.

Examine the related shunt pin selections if the keyset is connected to the hybrid port.

Examine the data transformer.

Examine the data modulation/de-modulation hybrid chip.

Examine the data transmit buffer 74HCT374.

Examine the data receiving buffer 74HCT244.

- Ⓒ Check the transformer T2 5692 on the keyset control board.

Good : Jump to the next step.

Fail : Replace the transformer T2 5692 on the keyset control board.

- Ⓓ Check the de-modulation process.

Good : Jump to the next step.

Fail : Repair the receiving circuit.

- Ⓔ Check the transmitting circuit.

Good : Jump to the next.

Fail : Repair the transmit circuit.

- Ⓕ Plug out/in the keyset again and check the operation. If fails again, replace CPU 80C51.

KEYSET KEY SCANNING FAILURE

- Ⓐ Check that all the buttons are not detected.

Good : Jump to the next step.

Fail : Examine the key board cable and re-connect.

Examine the key-scanning buffer U1 74HCT373 on the keyset key board.

- ⑥ Check that one row buttons are not detected.

Good : Jump to the next step.

Fail : Examine the related data bus connection from the control board to the scanning buffer U1 74HCT373 on the keyset key board.

- ⑦ Check that one column buttons are not detected.

Good : Jump to the next step.

Fail : Examine the related signal diode and replace it.

- ⑧ Examine the carbon contact and rubber. The key rubber can be replaceable but you should replace the key board if the carbon contact on the key board is out of order.

KEYSET LED DRIVING FAILURE

- ① Check the key board cable and the connections.

Good : Jump to the next step.

Fail : Re-connect the cable or replace it.

- ② Check that one row LED's can not be driven.

Good : Jump to the next step.

Fail : Examine the related row resistor and replace it.

Examine the row driver U2 74HCT373 on the keyset key board.

- ③ Check that one column LED's can not be driven.

Good : Jump to the next step.

Fail : Examine the column driver U3 UCN5801A.

- ④ Examine the LED and replace it.

KEYSET LCD DISPLAY FAILURE

- ① Check the LCD cable and the connections.

Good : Jump to the next step.

Fail : Re-connect the cable or replace it.

- ② Replace the LCD module.

KEYSET RING-TONE FAILURE

- Ⓐ Check that the speaker is driven.

Good : Jump to the next step.

Fail : Refer to the item related to speaker driving.

- Ⓑ Check CPU U1 80C51 pin 8 terminal.

Good : Trace the ring-tone path and replace the damaged part.

Fail : Replace the CPU U1 80C51.

KEYSET ALL SPEECH FAILURE

- Ⓐ Check the connections between the system and the keyset.

Good : Jump to the next step.

Fail : Connect correctly.

- Ⓑ Check the speech path in the keyset interface of the system during hook off

Good : Jump to the next step.

Fail : Examine the transformer ST-1C and the network.

- Ⓒ Check the speech transformer T1 on the keyset control board.

Good : Jump to the next step.

Fail : Replace the transformer T1 5692.

- Ⓓ Check the speech hybrid RX amplifier in RX failure

Good : Jump to the next step.

Fail : Repair the amplification circuit.

- Ⓔ Check the speech hybrid TX amplifier in TX failure.

Good : Jump to the next step.

Fail : Repair the amplification circuit.

- Ⓕ Examine the keyset network U4 CD22100 and replace it.

KEYSET HANDSET SPEECH FAILURE

- Ⓐ Check the handset assembly.

Good : Jump to the next step.

Fail : Replace the handset ass'y.

- Ⓑ Check the handset cord.

Good : Jump to the next step.

Fail : Replace the handset cord.

- Ⓒ Test the following items.

Handset TX failure : Examine the protection diode ZD1 1N4732A.

Handset RX failure : Examine the handset RX amplifier.

Handset Volume Control Failure : Examine the analog switch U7 4066.

Otherwise, check the network.

KEYSET SPEAKER-PHONE SPEECH FAILURE

- Ⓐ Check the speaker ass'y in the keyset in case of speaker-phone RX failure.

Good : Jump to the next step.

Fail : Examine the connections and repair it.

- Ⓑ Check the micro-phone ass'y in case of speaker-phone TX failure.

Good : Jump to the next step.

Fail : Examine the connections and repair it.

- Ⓒ Test the following items.

Examine the mute control analog switch U9D 4066.

Examine the network.

Examine the speaker-phone chip U10 MC34018.

Examine the speaker driver.

INDIVIDUAL LOUD BELL FAILURE

- Ⓐ Check the connections.

Good : Jump to the next step.

Fail : Connect correctly.

- Ⓑ Check the external amplifier and the speaker.

Good : Jump to the next step.

Fail : Replace the external amplifier and the speaker.

- Ⓒ Check the user program data. (Program code 36)

Good : Examine the amplifier circuit and the transformer.

Fail : Adjust the user program data.

VMS FEATURE FAILURE

- Ⓐ Check the user program data. (Program code 77, 16)

Good : Jump to the next step.

Fail : Adjust the user program data.

- Ⓑ Check the latch U14 74HCT373 on the keyset control board.

Good : Jump to the next step.

Fail : Replace U14 74HCT373.

- Ⓒ Check the DRAM memories.

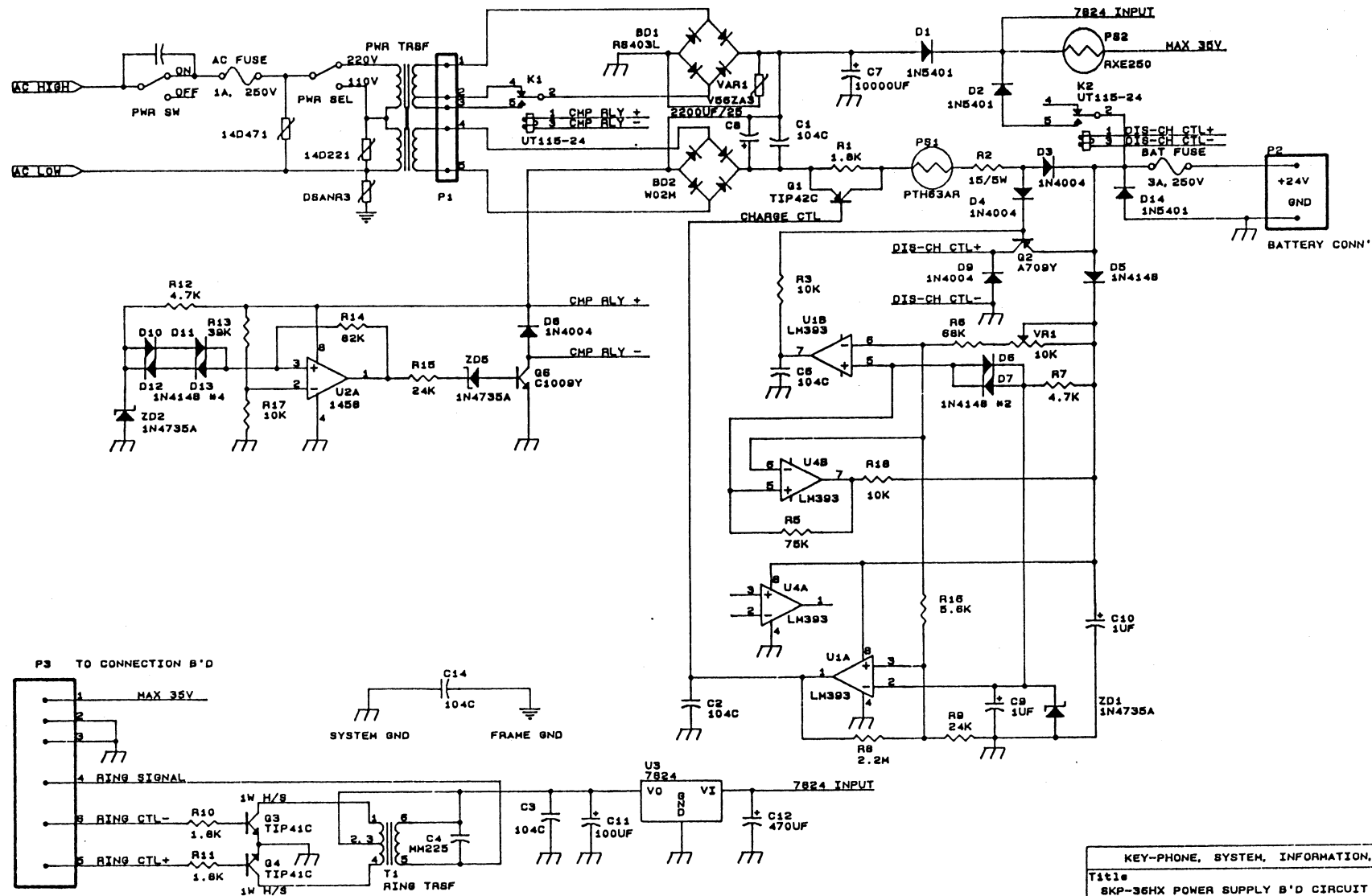
Good : Replace the VMS processor U16 KS5917 on the keyset control board.

Fail : Replace the damaged DRAM.

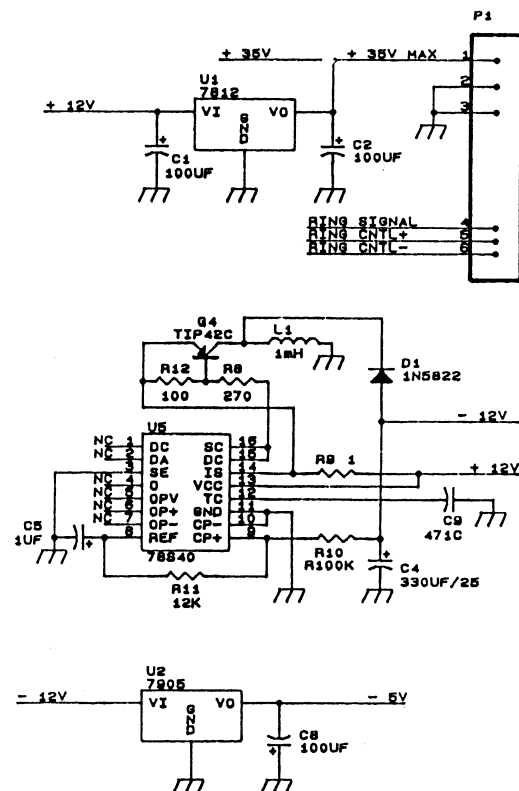
3 . C I R C U I T D I A G R A M

C O N T E N T S

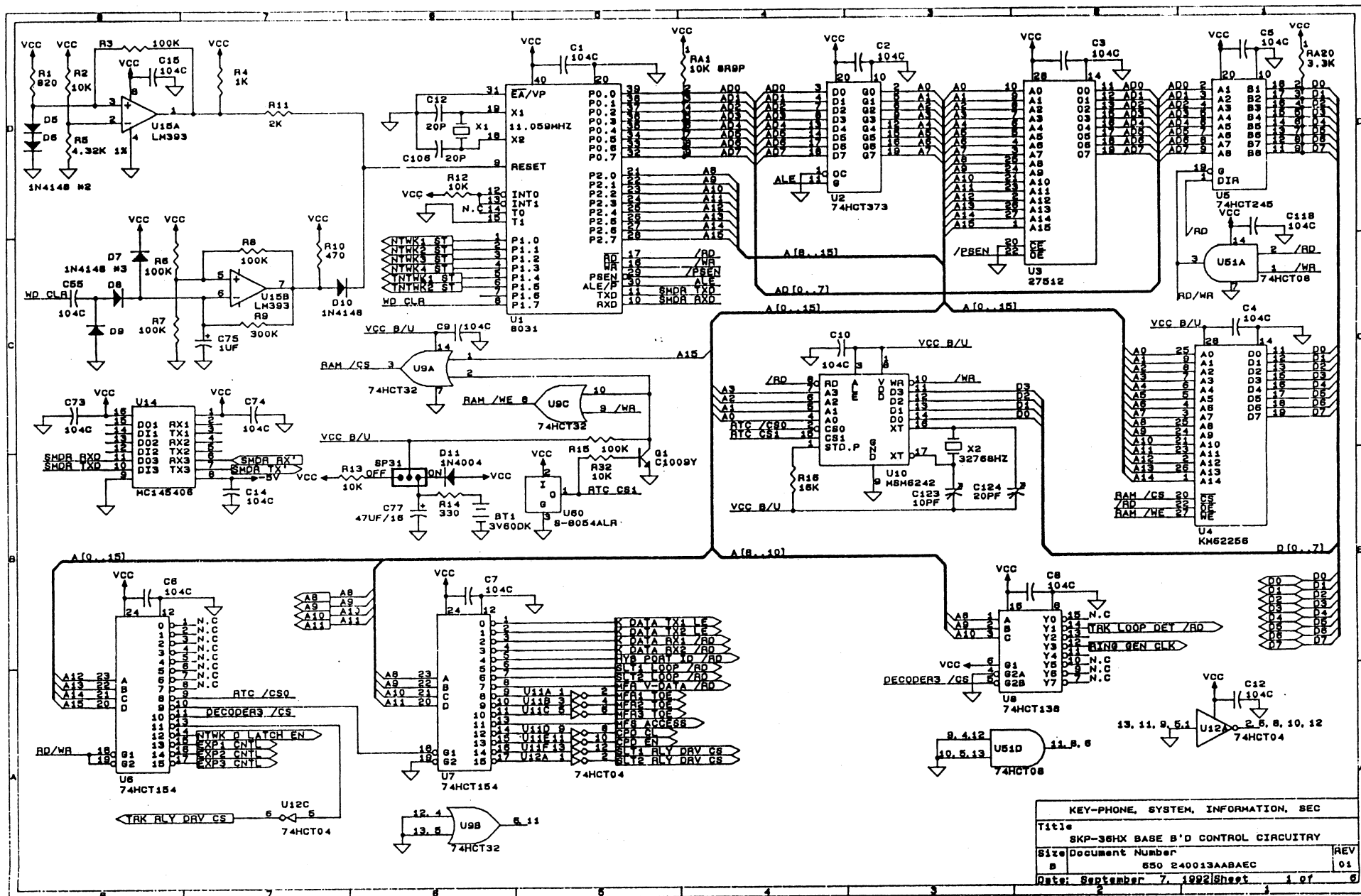
Power Supply Board Circuit Diagram	213
Connection Board Circuit Diagram	214
Base Board Control Part Circuit Diagram	215
Base Board Network & MFR Part Circuit Diagram	216
Base Board Additional Part Circuit Diagram	217
Base Board Keyset & Hybrid Interface Circuit Diagram ...	218
Base Board Trunk & SLT Interface Circuit Diagram	219
Base Board Connection Informations	220
4MSLC Expansion Board Circuit Diagram	221
4SLC Expansion Board Circuit Diagram	222
2CO/2HLC Expansion Board Circuit Diagram	223
UNIV-A Expansion Board Circuit Diagram	224
UNIV-B Expansion Board Circuit Diagram	225
Door-phone Circuit Diagram	226
AS-11/30B, E, BV, EV Control Board Circuit Diagram A ...	227
AS-11/30B, E, BV, EV Control Board Circuit Diagram B ...	228
AS-11/30B, E, BV, EV Control Board Circuit Diagram C ...	229
AS-11/30B, E, BV, EV Key Board Circuit Diagram	230

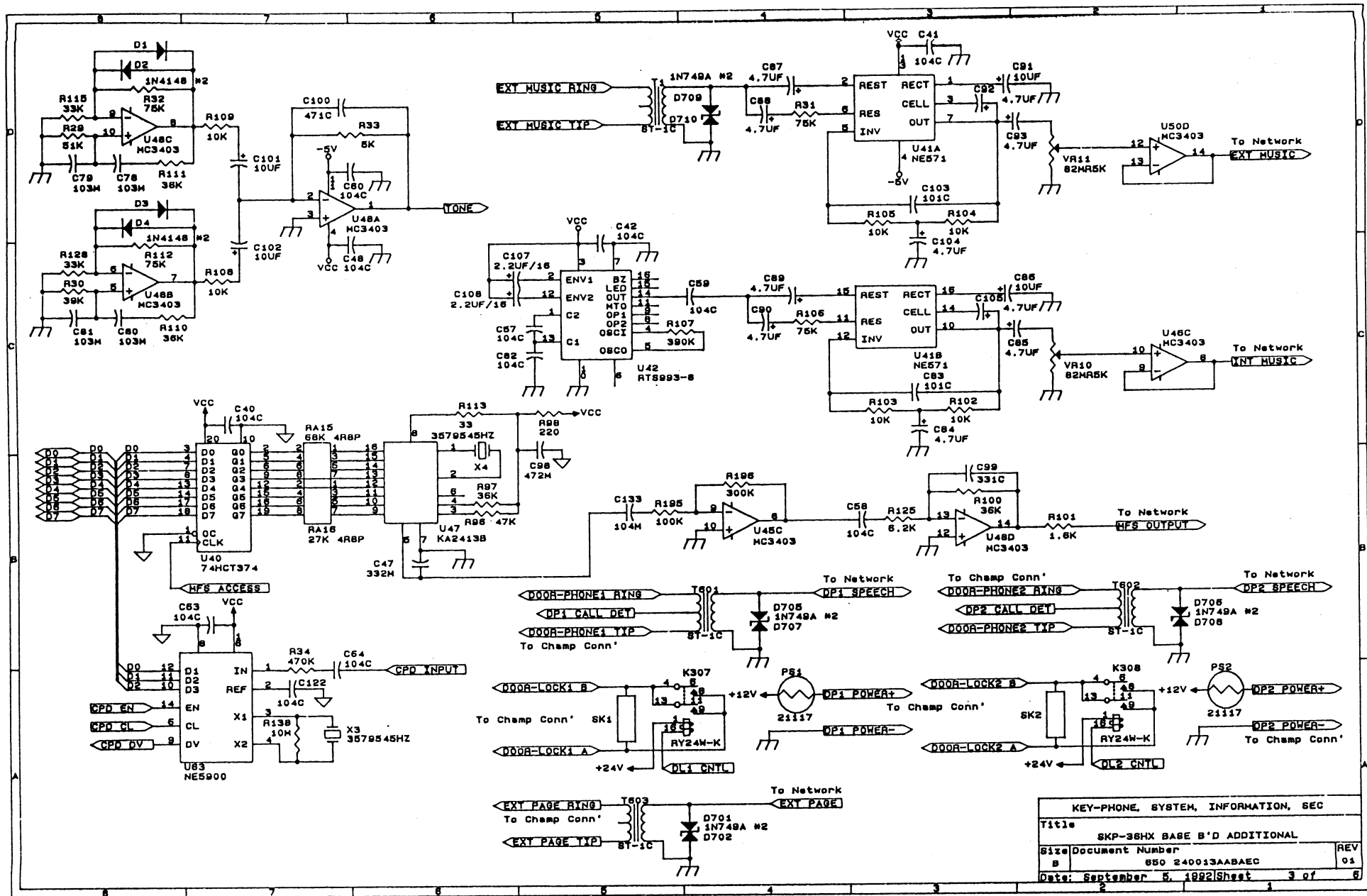


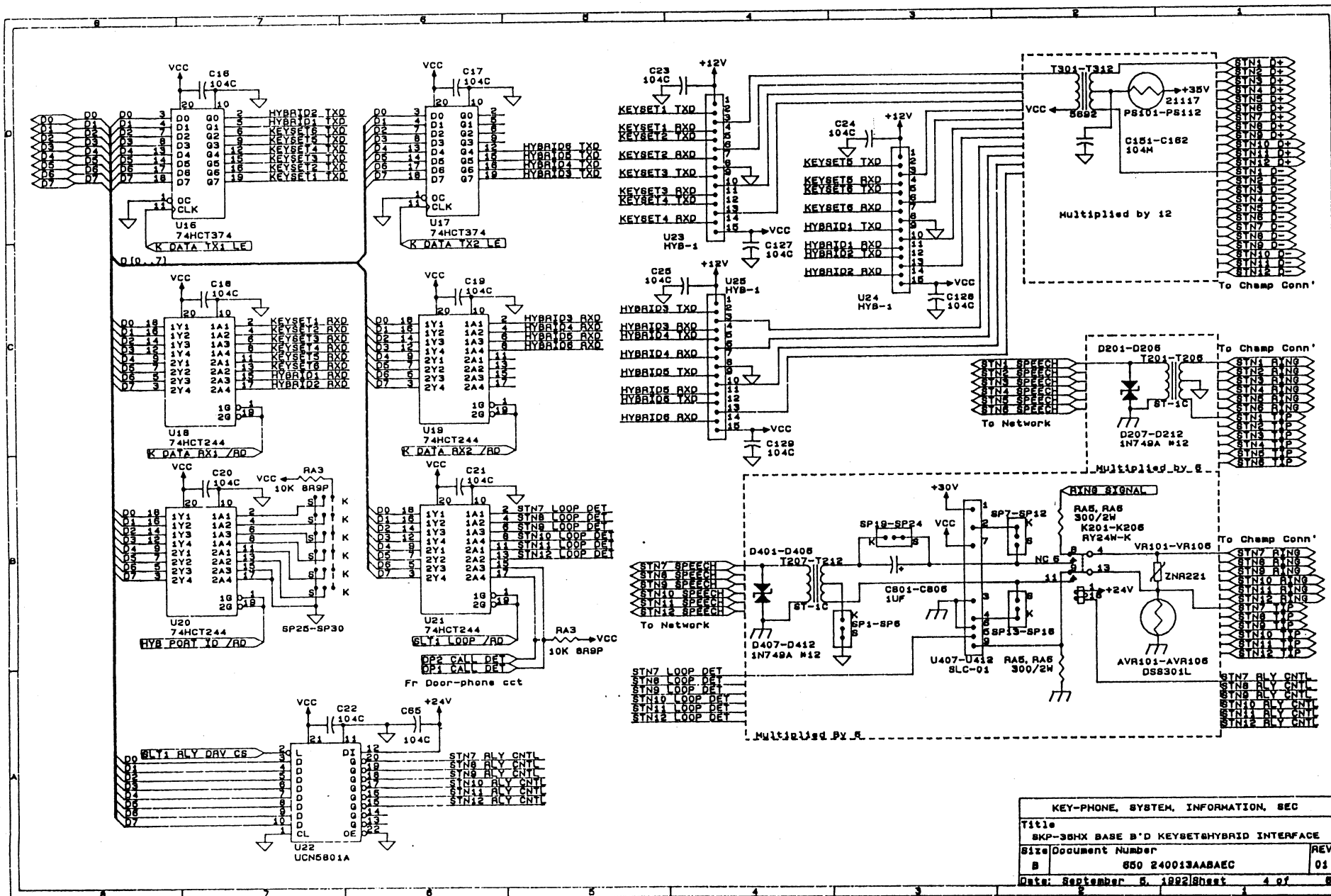
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Sheet	1 of	1

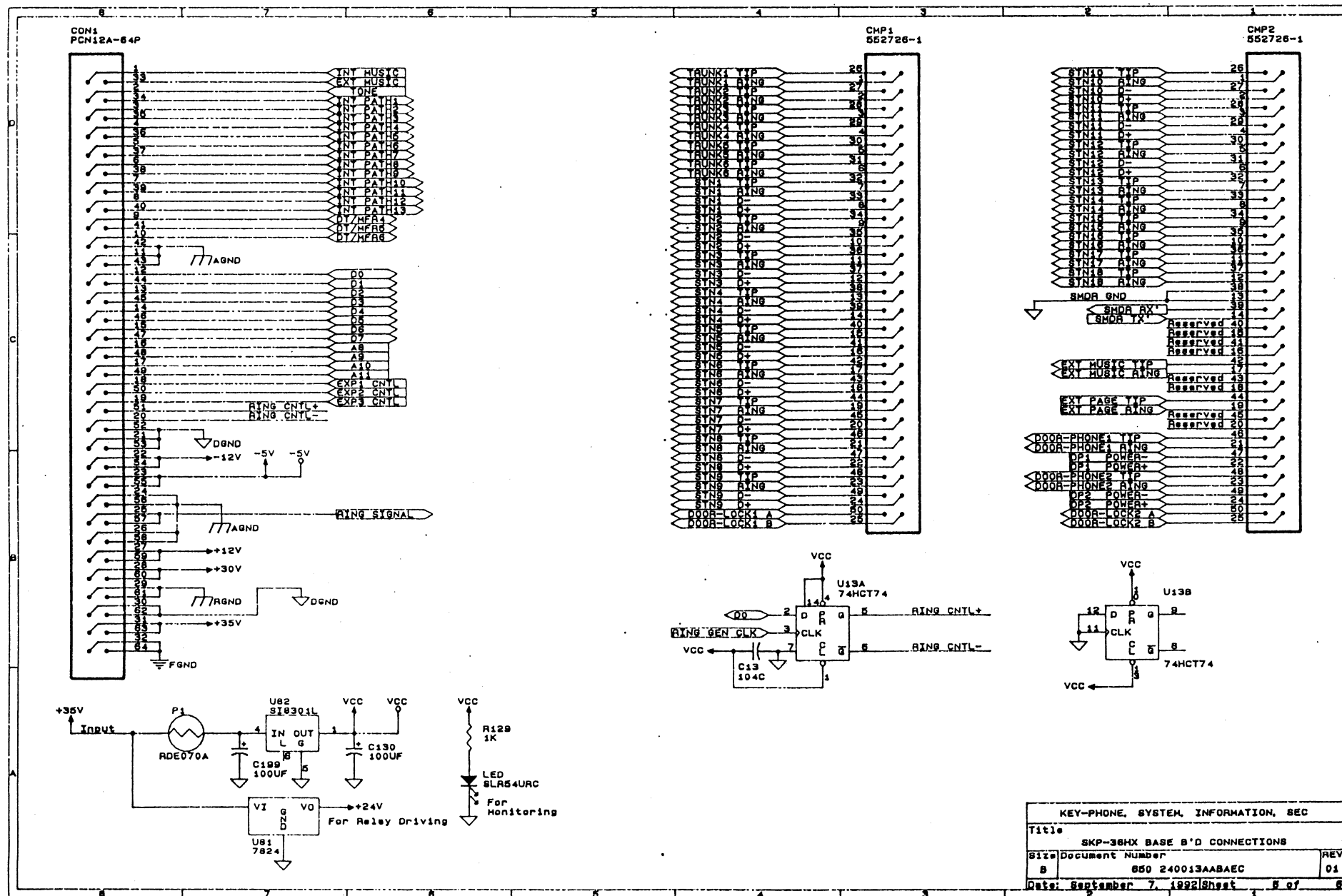


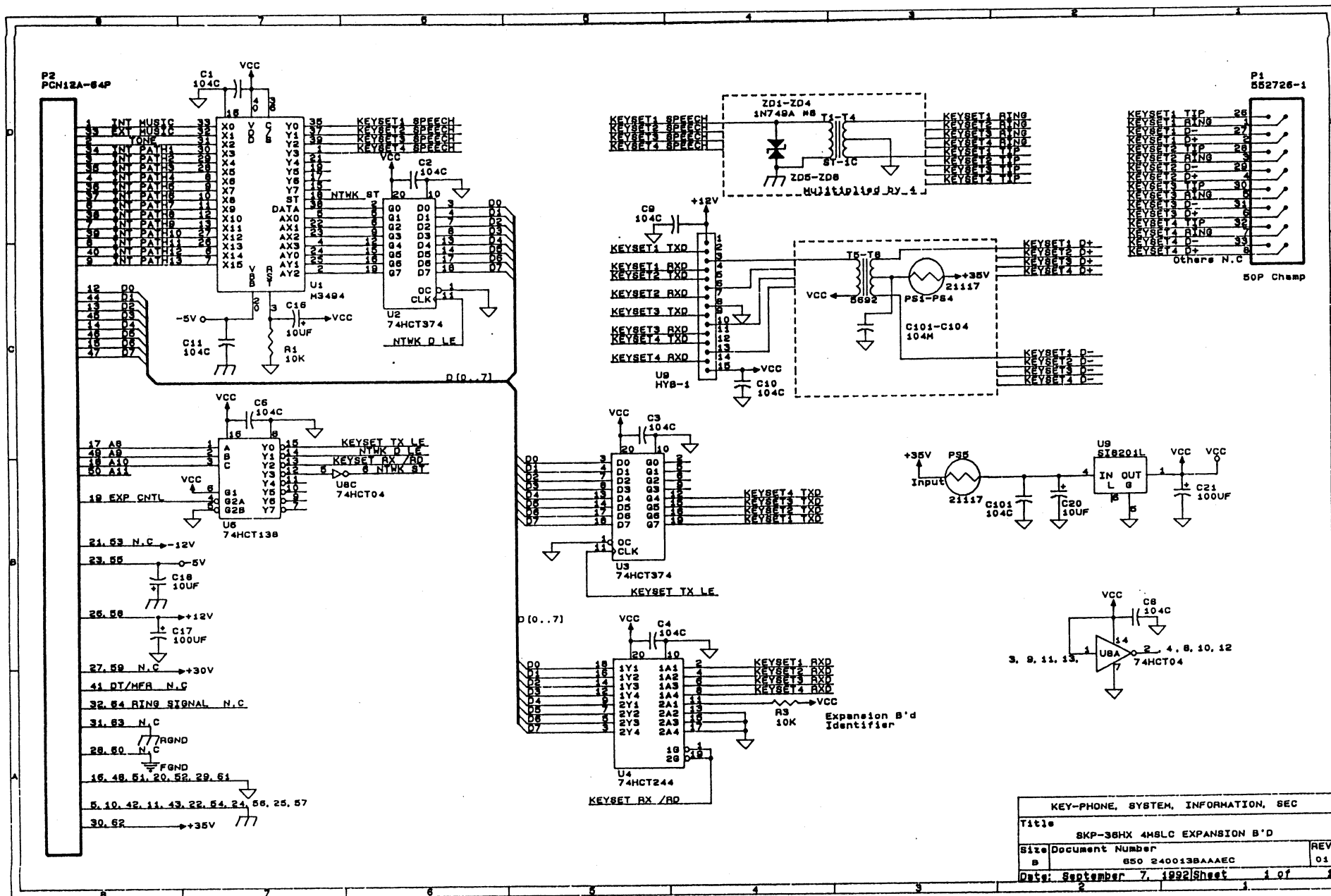
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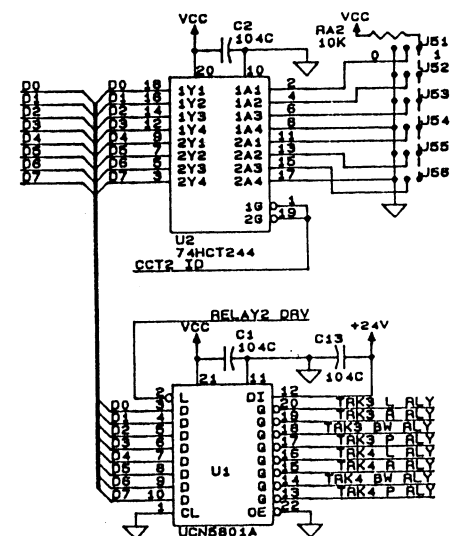
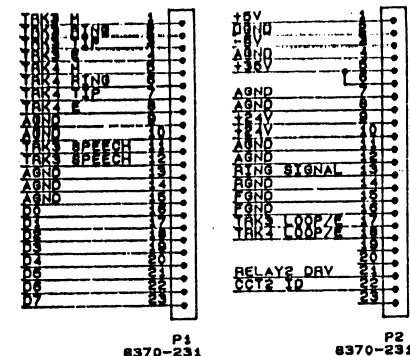




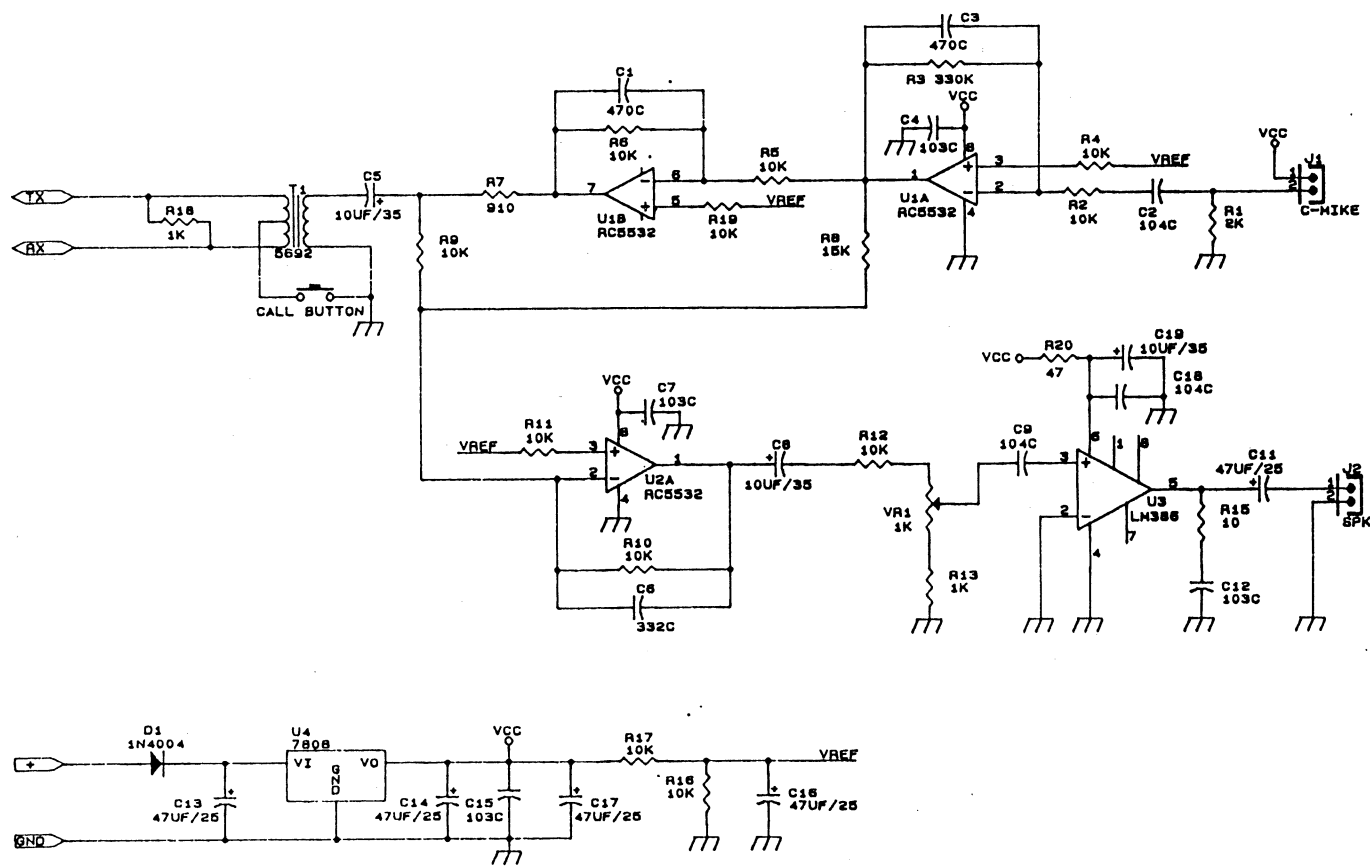




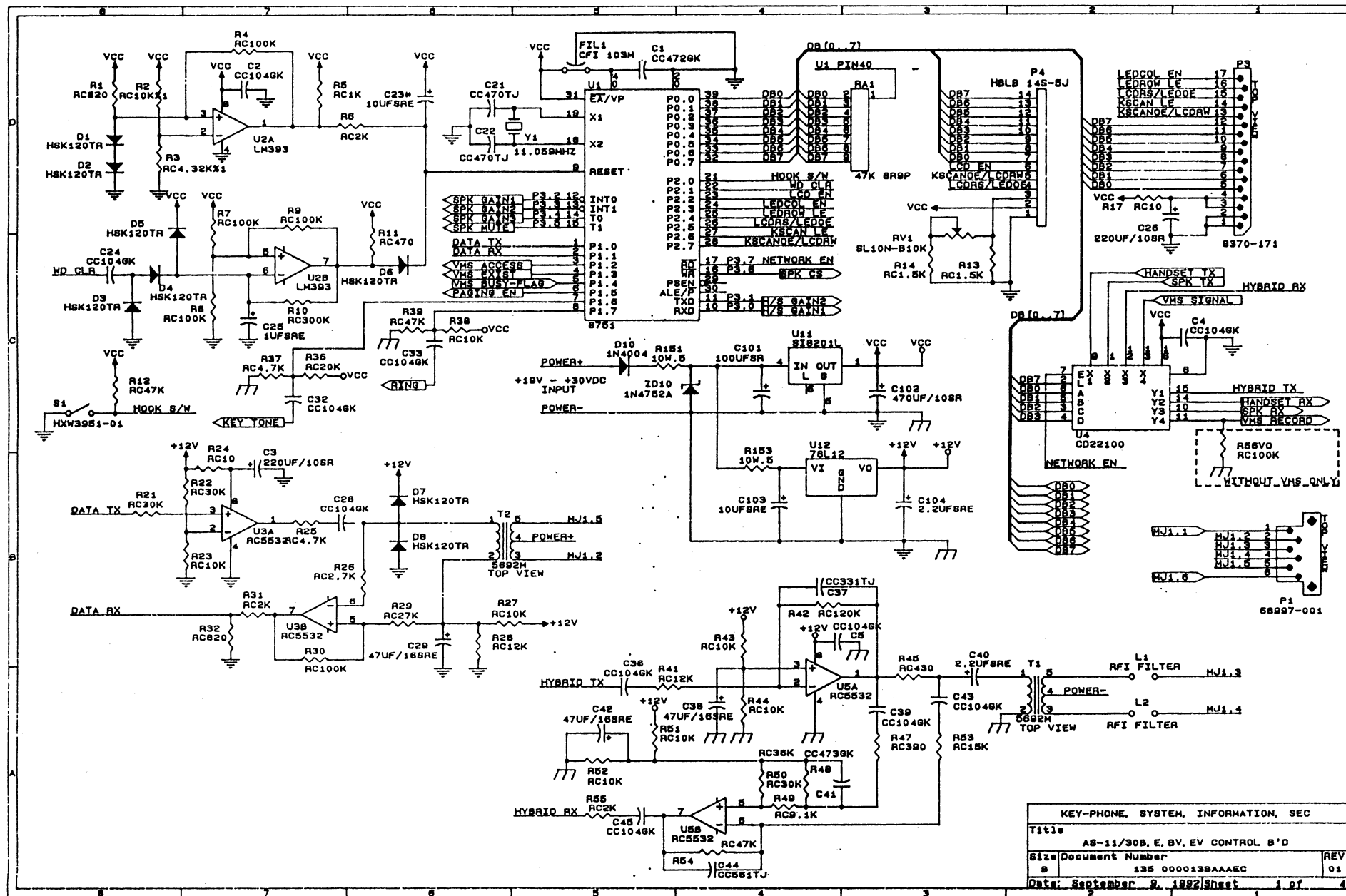


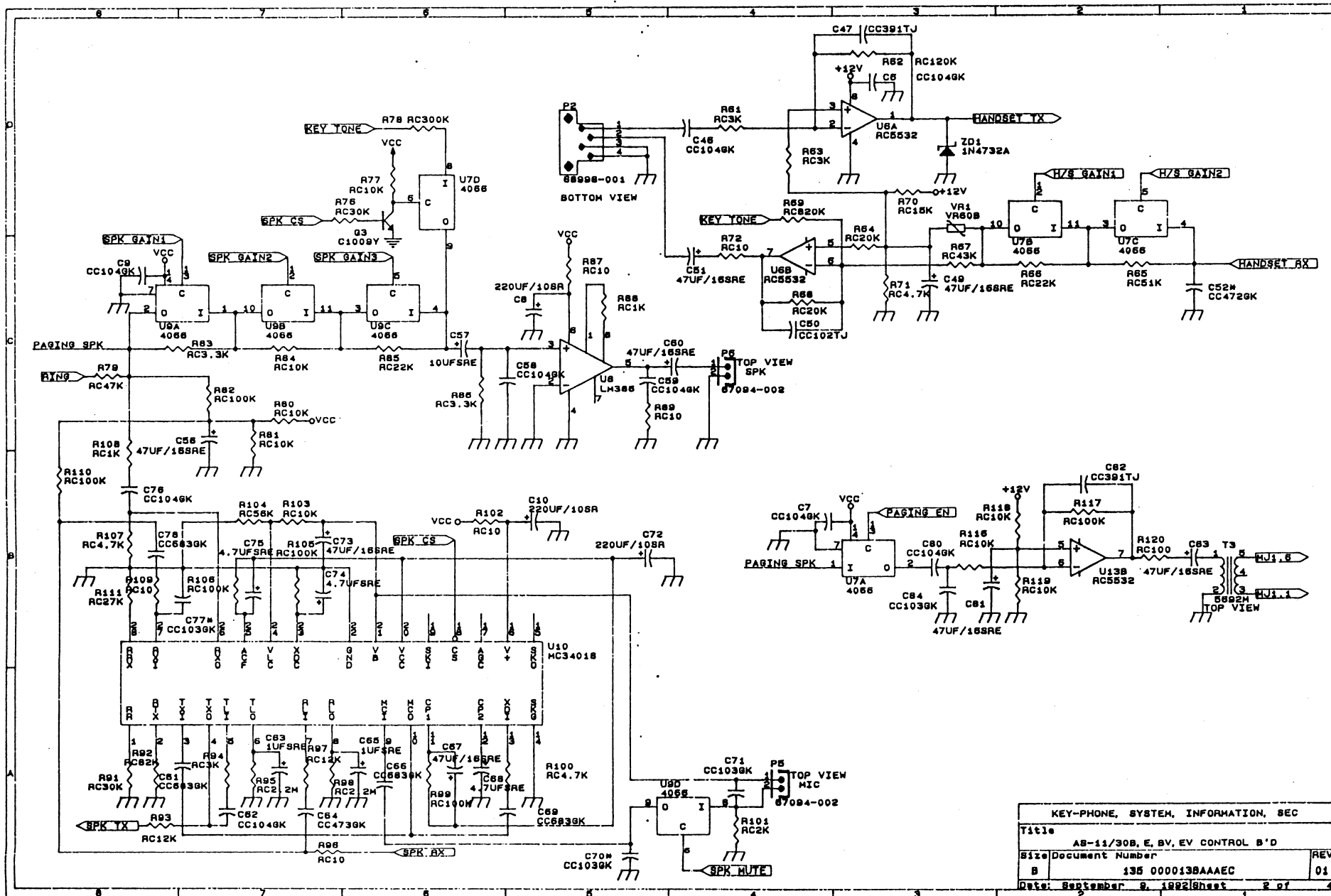


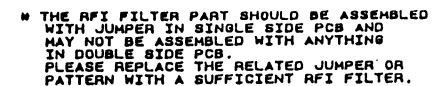
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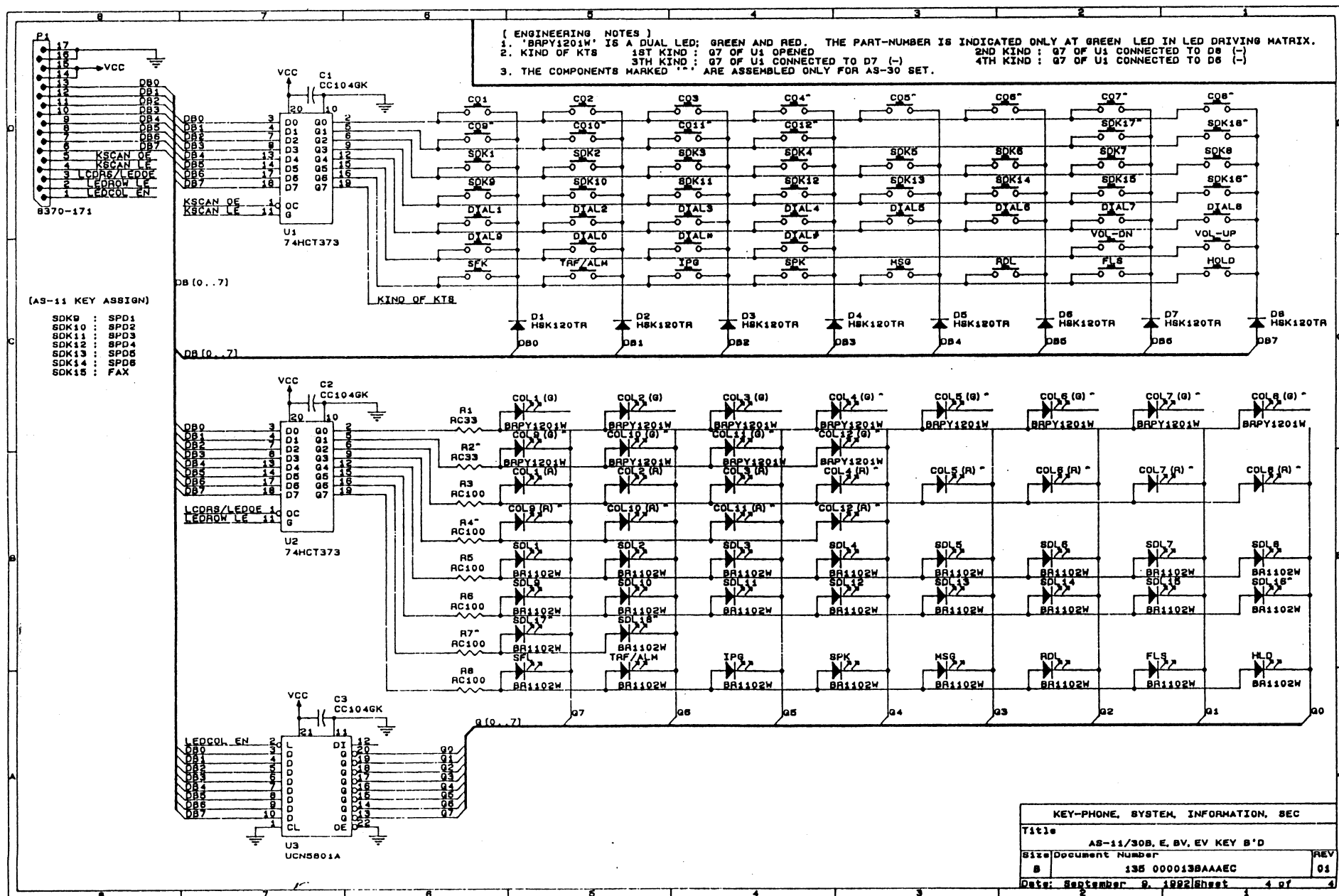


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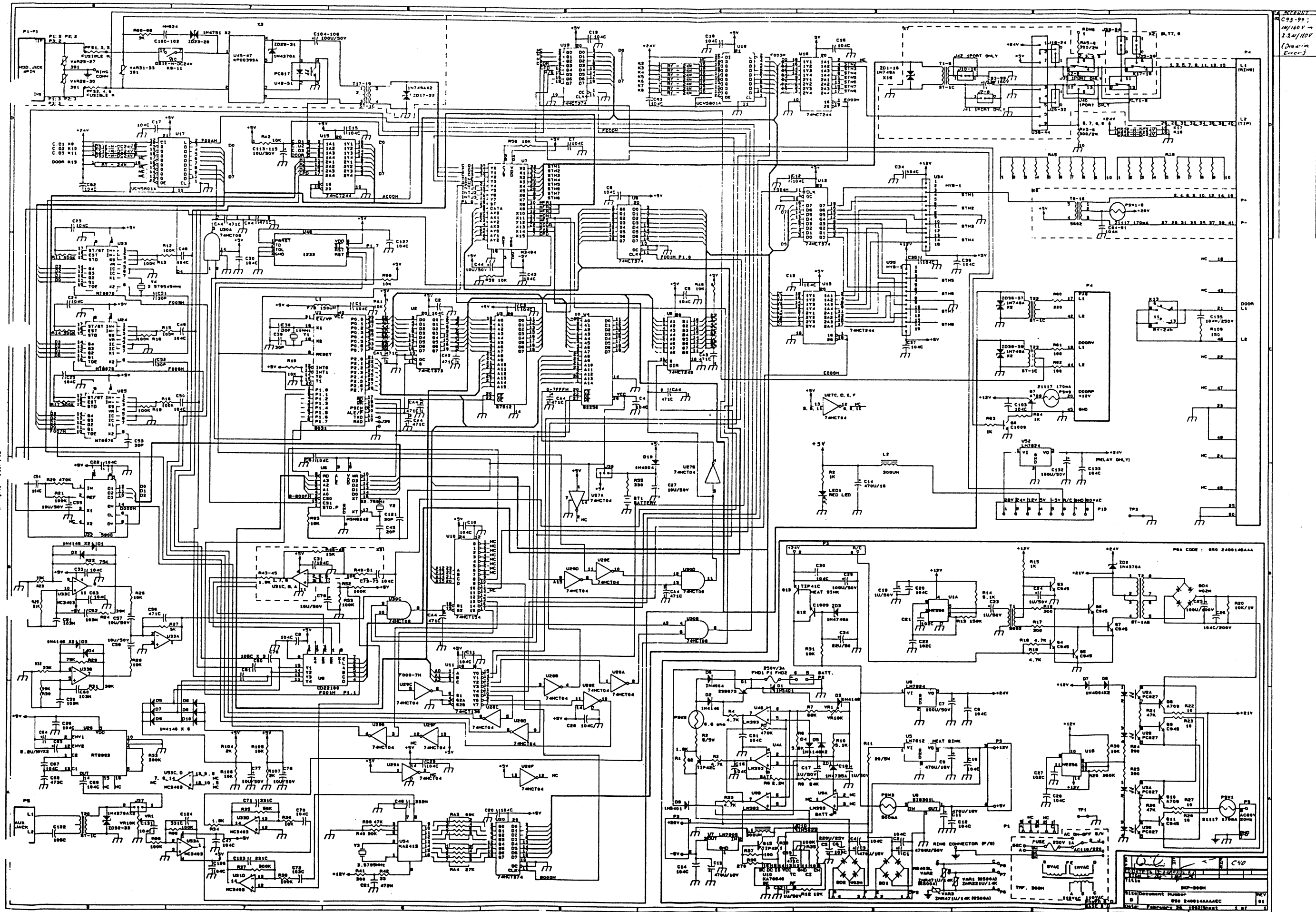








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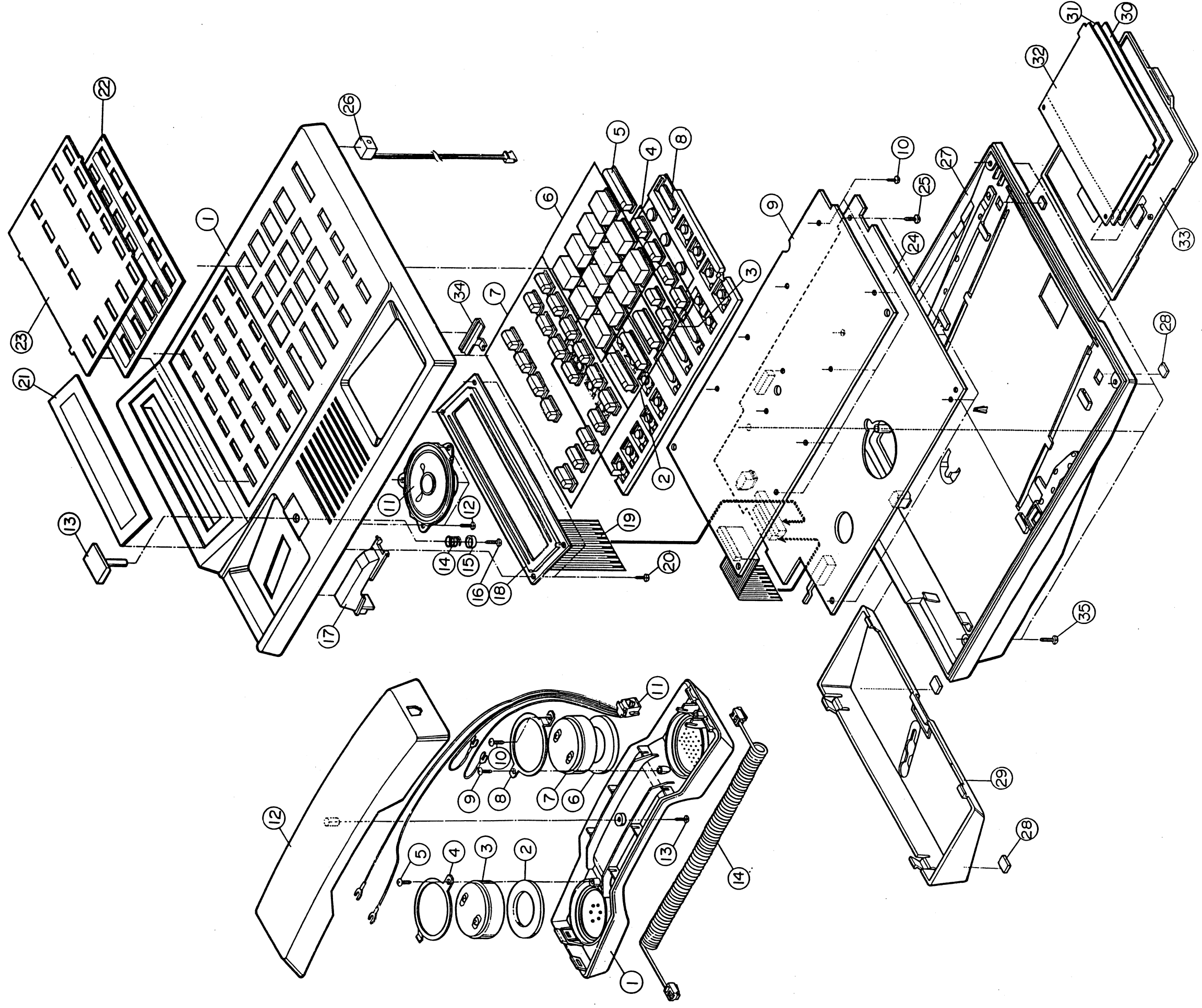


CS9-99
10/100V
2.24/100V
(Power Error)

PSA CODE: 850 2400148AAA

REV 01
DATE 01/01/00
FABRICATE 01/01/00

5. KEYSET EXPLODED VIEW



1. BASIC KSU EXPLODED VIEW

